



MMIC SURFACE MOUNT

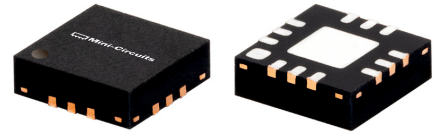
Low Noise Amplifier

TSS-66921LN+

50Ω 660 to 920 MHz Shutdown Feature

THE BIG DEAL

- Ultra-Low Noise Figure, Typ. 1.0 dB
- High P1dB, Typ. +16.3 dBm
- High OIP3, Typ. +25.4 dBm
- High Input Power Handling, Max +24 dBm
- Shutdown Feature
- Single Supply Voltage, +3.3 V
- 3x3 mm, 12-Lead QFN-Style Package

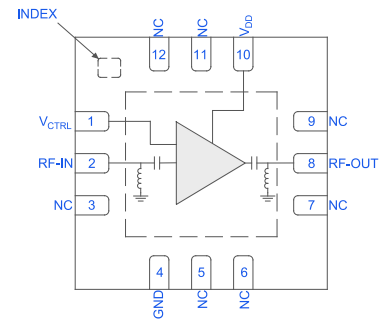


Generic photo used for illustration purposes only

APPLICATIONS

- 5G MIMO Radio Systems
- Radar, EW, and ECM Defense Systems
- ISM

FUNCTIONAL DIAGRAM



PRODUCT OVERVIEW

The TSS-66921LN+ is a pHEMT-based wideband, ultra-low noise MMIC amplifier with high IP3, flat gain, and voltage-controlled shutdown capability. Operating from 660 to 920 MHz, this amplifier features typical 1.1 dB noise figure, 35.0 dB gain, +16.3 dBm P1dB, and +25.4 dBm OIP3. This combination of characteristics makes it ideal for sensitive receiver applications. The device is internally DC blocked, and a DC path to ground is present at the RF input and output ports for ESD protection. TSS-66921LN+ operates on a single +3.3 V supply and comes in a small, low profile, 3x3 mm QFN-style package for ease of integration into dense circuit board layouts.

KEY FEATURES

| Features | Advantages |
|-------------------------------------|--|
| Ultra-Low Noise Figure, Typ. 1.1 dB | Operating from a single supply, this ultra-low noise MMIC enables low system noise figure performance without the need for complicated discrete-based solutions. |
| High Gain, Typ. 35.0 dB | The MMIC amplifier's high gain enables fewer system components in receiver signal chains. |
| Shutdown Feature | A voltage-controlled shutdown feature allows the part to be quickly disabled to conserve power when not in use. |
| 3x3 mm 12-Lead QFN-Style Package | Small footprint saves space in dense layouts while providing low inductance, repeatable transitions, and excellent thermal contact to the PCB. Industry standard packaging allows for ease of assembly in high volume manufacturing processes. |



MMIC SURFACE MOUNT

Low Noise Amplifier

TSS-66921LN+

50Ω 660 to 920 MHz Shutdown Feature

ELECTRICAL SPECIFICATIONS¹ AT 25°C, V_{DD} = +3.3 V

| Parameter | Condition (MHz) | Amplifier - ON (V _{CTRL} = 0 V) | | | Amplifier - OFF (V _{CTRL} = +1.5 V) | Units |
|---|-----------------|---|--------|------|---|-------|
| | | Min. | Typ. | Max. | Typ. | |
| Frequency Range | | 660 | | 920 | 660 - 920 | MHz |
| Gain | 660 | 33.3 | 34.9 | | -45.4 | dB |
| | 780 | 33.4 | 35.0 | | -46.4 | |
| | 920 | 33.0 | 34.6 | | -40.8 | |
| Input Return Loss | 660 | | 15 | | | dB |
| | 780 | | 20 | | | |
| | 920 | | 20 | | | |
| Output Return Loss | 660 | | 18 | | | dB |
| | 780 | | 20 | | | |
| | 920 | | 16 | | | |
| Isolation | 660-920 | | 62 | | 44 | dB |
| Output Power at 1dB Compression (P _{1dB}) | 660 | | +16.0 | | | dBm |
| | 780 | | +16.3 | | | |
| | 920 | | +16.0 | | | |
| Output Third-Order Intercept Point (P _{OUT} = 0 dBm/Tone) | 660 | | +26.1 | | | dBm |
| | 780 | | +25.4 | | | |
| | 920 | | +25.2 | | | |
| Noise Figure | 660 | | 1.0 | | | dB |
| | 780 | | 1.1 | | | |
| | 920 | | 1.0 | | | |
| ON Time (50% V _{CTRL} to 90% RF) | | | 140.0 | | | ns |
| RISE Time (10% RF to 90% RF) | | | 87.6 | | | ns |
| FALL Time (90% RF to 10% RF) | | | 17.0 | | | ns |
| OFF Time (50% V _{CTRL} to 10% RF) | | | 31.6 | | | ns |
| Device Operating Voltage (V _{DD}) | | +3 | +3.3 | +3.5 | +3.3 | V |
| Device Operating Current (I _{DD}) ² | | | 58.4 | 68 | 0 | mA |
| Device Control Voltage (V _{CTRL}) | | | 0 | | +1.5 | V |
| Device Control Current (I _{CTRL}) | | | 3 | | 4 | mA |
| DC Current Variation vs. Temperature ³ | | | -26.67 | | | μA/°C |
| DC Current Variation vs. Voltage ⁴ | | | 12.4 | | | μA/mV |

1. Tested on Mini-Circuits Characterization Test Board TB-TSS66921LNC+. See Figure 2. Board loss de-embedded to the device.

2. Current at P_{IN} = -35 dBm.

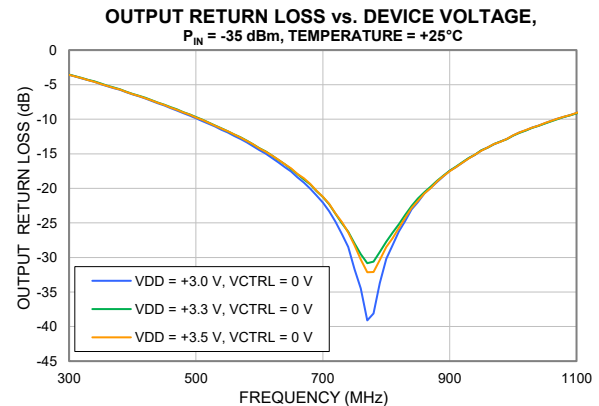
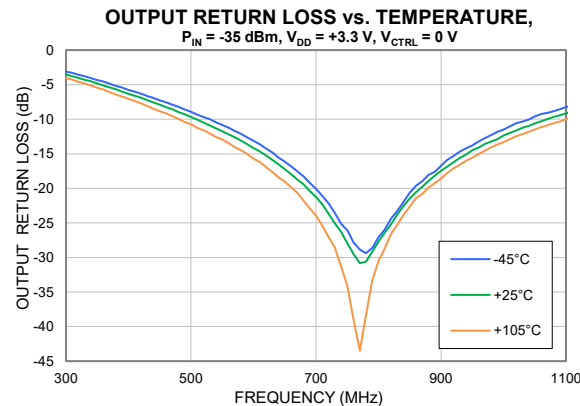
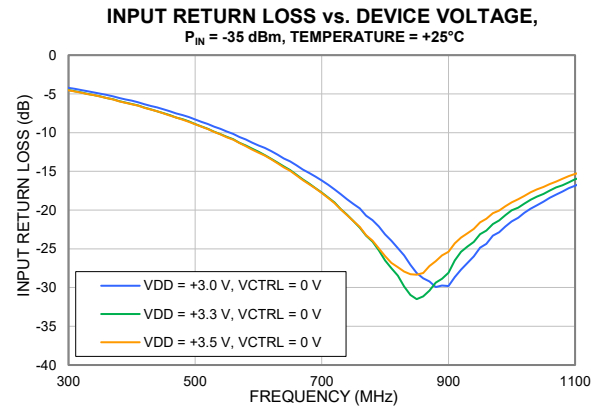
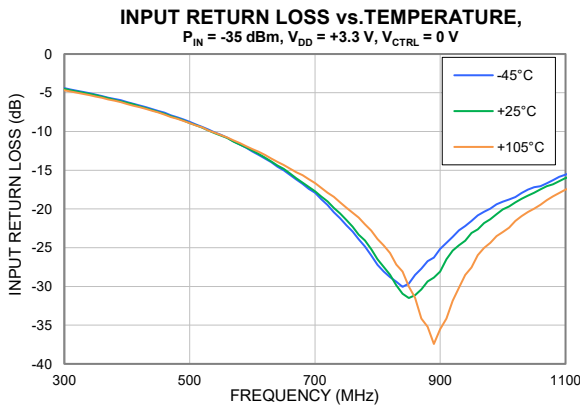
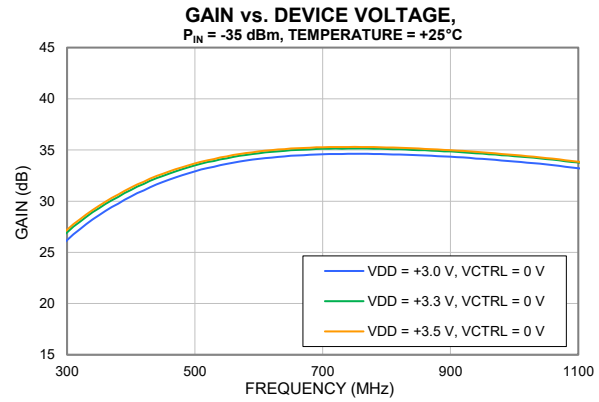
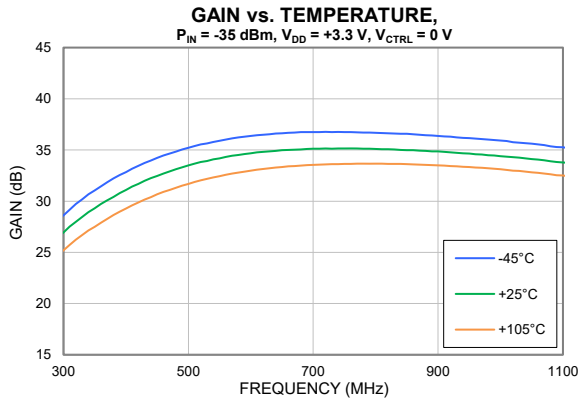
3. (Current at +105°C - Current at -45°C) / (+150°C)

4. (Current at +3.5 V - Current at +3.0 V) / (+0.5 V)



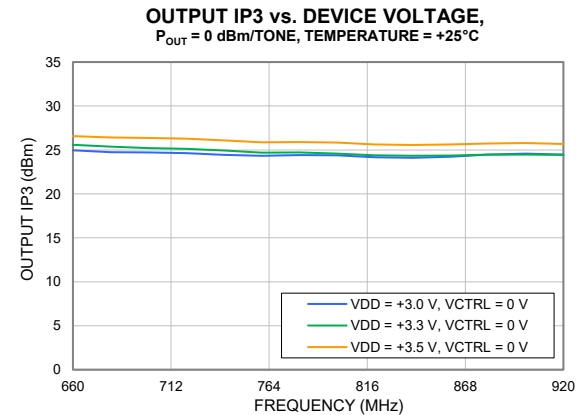
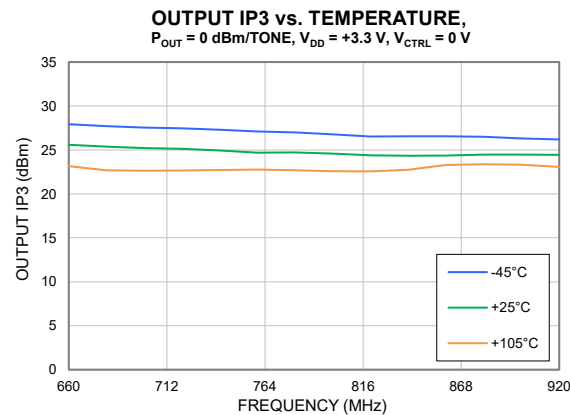
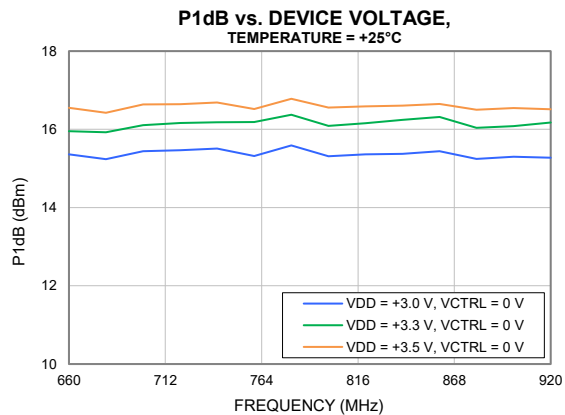
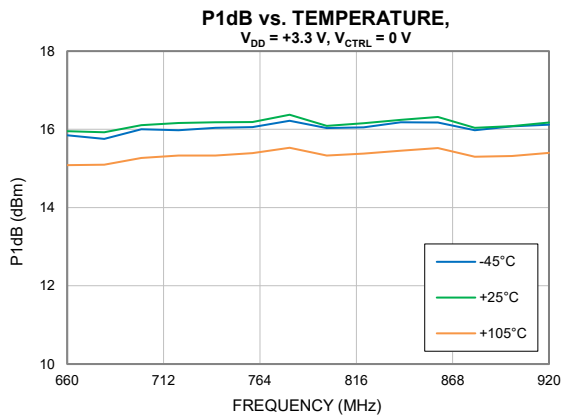
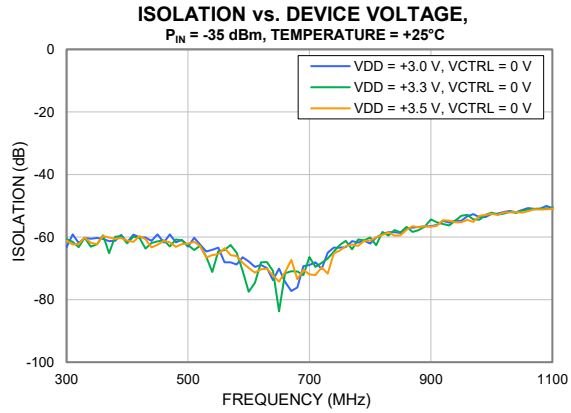
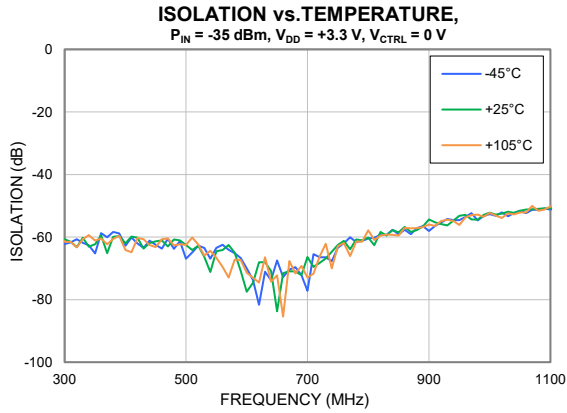


TYPICAL PERFORMANCE GRAPHS



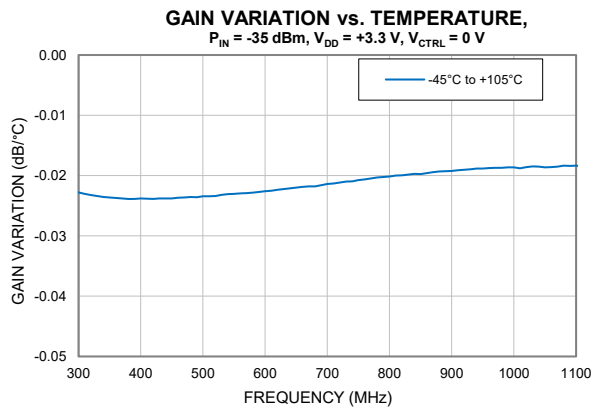
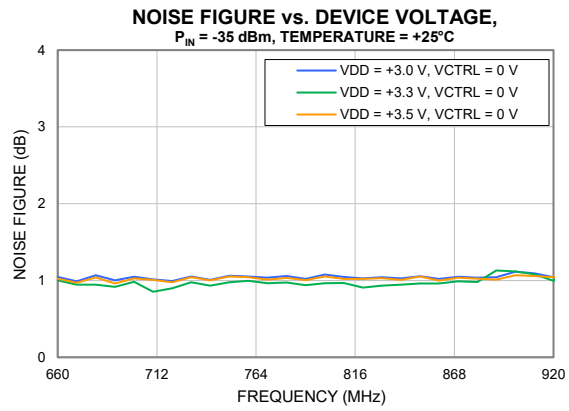
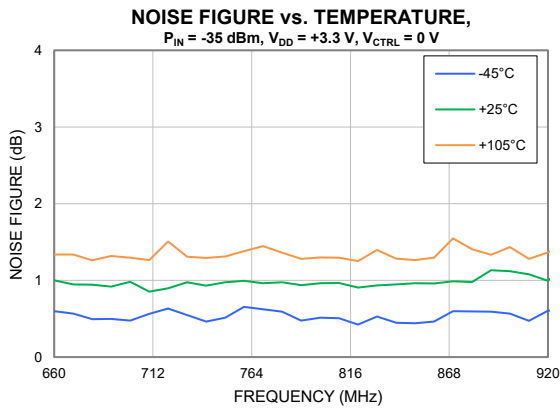


TYPICAL PERFORMANCE GRAPHS





TYPICAL PERFORMANCE GRAPHS



ABSOLUTE MAXIMUM RATINGS⁵

| Parameter | Ratings |
|--|-----------------|
| Operating Temperature | -45°C to +105°C |
| Storage Temperature | -65°C to +150°C |
| Junction Temperature ⁶ | +150°C |
| Total Power Dissipation | 0.67 W |
| Input Power (CW), $V_{DD} = +3.3$ V $V_{CTRL} = 0$ V: | +24 dBm |
| DC Voltage at V_{DD} $V_{CTRL} = 0$ V: | +5 V |
| $V_{CTRL} = +1.5$ V: | +5 V |
| DC Current I_{DD} $V_{CTRL} = 0$ V: | 150 mA |
| $V_{CTRL} = +1.5$ V: | 20 mA |
| DC Voltage at V_{CTRL} $V_{DD} = +3.3$ V: | +5 V |
| DC Current I_{CTRL} $V_{DD} = +3.3$ V: | 10 mA |

5. Permanent damage may occur if any of these limits are exceeded. Maximum ratings are not intended for continuous normal operation.

6. Peak temperature on top of Die.

CONTROL VOLTAGE (V_{CTRL})

| Amplifier State | Min. | Typ. | Max. | Units |
|-----------------|------|------|------|-------|
| Amplifier – ON | 0 | 0 | +0.2 | V |
| Amplifier – OFF | +1 | +1.5 | +5 | V |

THERMAL RESISTANCE

| Parameter | Ratings |
|---|----------|
| Thermal Resistance (θ_{JC}) ⁷ | 67.4°C/W |

7. θ_{JC} = (Hot Spot Temperature on Die - Temperature at Ground Lead)/Dissipated Power

ESD RATING

| | Class | Voltage Range | Reference Standard |
|-----|-------|------------------|-----------------------------|
| HBM | 1A | 250 V to < 500 V | ANSI/ESDA/JEDEC JS-001-2023 |
| CDM | C3 | ≥ 1000 V | ANSI/ESDA/JEDEC JS-002-2022 |



ESD HANDLING PRECAUTION: This device is designed to be Class 1A for HBM. Static charges may easily produce potentials higher than this with improper handling and can discharge into DUT and damage it. As a preventive measure Industry standard ESD handling precautions should be used at all times to protect the device from ESD damage.

MSL RATING

Moisture Sensitivity: MSL1 in accordance with IPC/JEDEC J-STD-020E /JEDEC J-STD-033C



FUNCTIONAL DIAGRAM

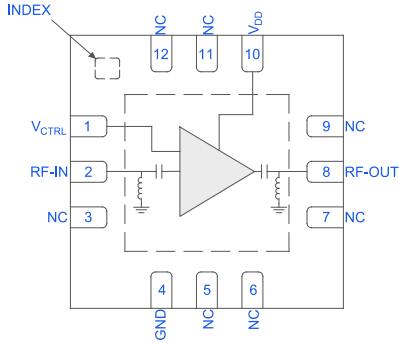


Figure 1. TSS-66921LN+ Functional Diagram

PAD DESCRIPTION

| Function | Pad Number | Application Description (Refer to Figure 2) |
|-------------------|------------------|---|
| V _{CTRL} | 1 | DC Input Pad connects to control voltage port V _{CTRL} . |
| RF-IN | 2 | RF-IN Pad connects to RF Input port. |
| RF-OUT | 8 | RF-OUT Pad connects to RF Output port. |
| V _{DD} | 10 | DC Input Pad connects to voltage input port V _{DD} . |
| NC | 3,5-7,9,11 | Not used internally. Connected to ground on test board. |
| NC ^s | 12 | Do not connect to ground on PCB. Pad is used internally. |
| GND | 4, Paddle, Index | Connects to ground. |

8. Pin 12 is used internally to the DUT. Connecting Pin 12 externally can cause permanent damage to the DUT.

CHARACTERIZATION TEST BOARD

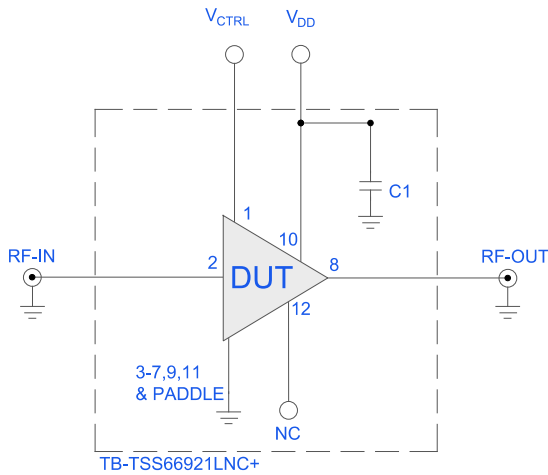


Figure 2. TSS-66921LN+ Characterization and Application Circuit.

Electrical Parameters and Conditions

Gain, Return Loss, Output Power at 1dB Compression (P1dB), Output IP3 (OIP3), and Noise Figure measured using N5242A PNA-X microwave network analyzer.

Conditions:

- 1) Gain and Return Loss: P_{IN} = -35 dBm
- 2) Output IP3 (OIP3): Two tones, spaced 1 MHz apart, 0 dBm/Tone at output.
- 3) V_{DD} = +3.3 V

| Component | Value | Size | Part Number | Manufacturer |
|-----------|-------|------|--------------------|--------------|
| C1 | 1 μF | 0402 | GRM155C81E105KE11D | Murata |

Power ON/Power OFF Sequence:

Caution: Permanent damage to the device will occur if the Power ON and Power OFF sequences are not followed.

POWER ON:

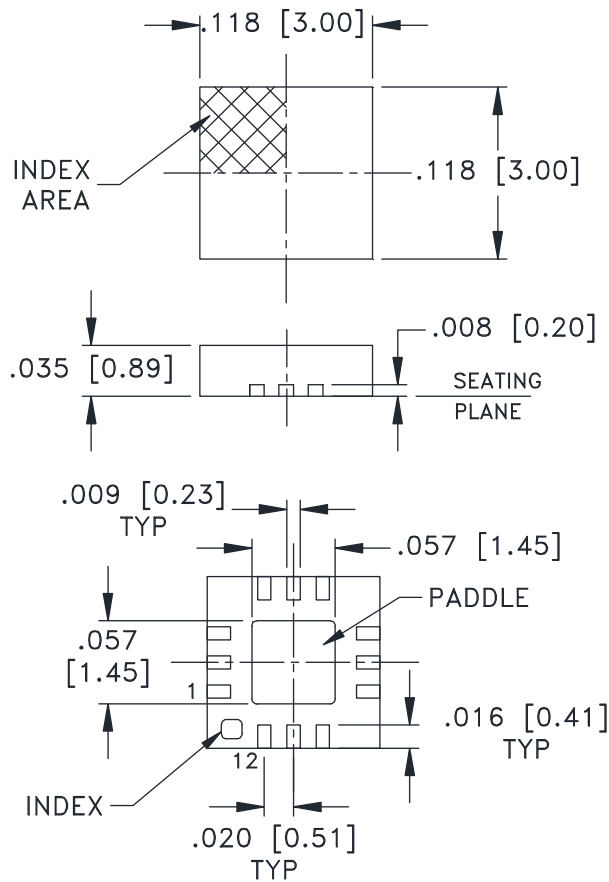
- 1) Set V_{DD} to +3.3 V
- 2) Turn on V_{DD}
- 3) Set V_{CTRL} to 0 V
- 4) Turn on V_{CTRL}
- 5) Apply RF Signal.

POWER OFF:

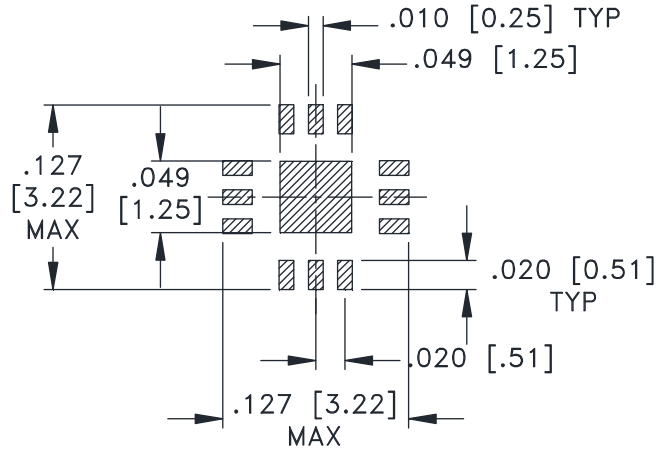
- 1) Turn off RF Signal.
- 2) Turn off V_{CTRL}
- 3) Turn off V_{DD}



CASE STYLE DRAWING



PCB Land Pattern

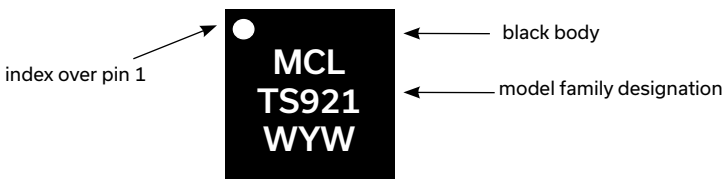


SUGGESTED LAYOUT,
TOLERANCE TO BE WITHIN ±.002

Weight: .02 Grams

Dimensions are in inches [mm]. Tolerances in inches: 2 Pl. ±.01; 3 Pl.±.004

PRODUCT MARKING



Marking may contain other features or characters for internal lot control



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TSS-66921LN+

50Ω 660 to 920 MHz Shutdown Feature

ADDITIONAL DETAILED INFORMATION IS AVAILABLE ON OUR DASHBOARD

[CLICK HERE](#)

| | |
|--|---|
| Performance Data & Graphs | Data Graphs S-Parameter (S2P Files) Data Set (.zip file) |
| Case Style | DQ1225 Plastic package, exposed paddle, Lead Finish: Matte-Tin |
| RoHS Status | Compliant |
| Tape & Reel Standard quantities available on reel | F66 7" reels with 20, 50, 100, 200, 500, 1K, 2K, or 3K devices |
| Suggested Layout for PCB Design | PL-807 |
| Evaluation Board | TB-TSS66921LNC+ Gerber File |
| Environmental Ratings | ENV08T1 |

NOTES

- A. Performance and quality attributes and conditions not expressly stated in this specification document are intended to be excluded and do not form a part of this specification document.
- B. Electrical specifications and performance data contained in this specification document are based on Mini-Circuits' applicable established test performance criteria and measurement instructions.
- C. The parts covered by this specification document are subject to Mini-Circuits standard limited warranty and terms and conditions (collectively, "Standard Terms"); Purchasers of this part are entitled to the rights and benefits contained therein. For a full statement of the standard terms and the exclusive rights and remedies thereunder, please visit Mini-Circuits' website at www.minicircuits.com/terms/viewterm.html

