MMIC DIE

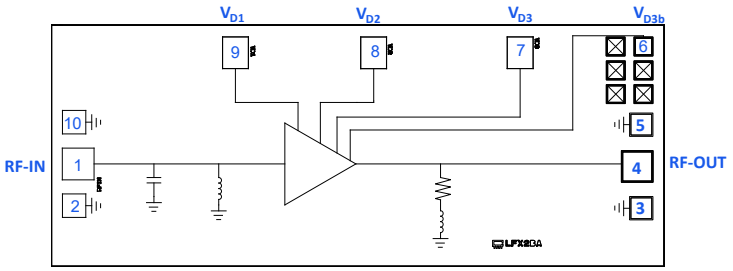
Low Noise Amplifier PMA4-8243LN-D+

50Ω 8 to 24 GHz Wideband Amplifier

THE BIG DEAL

- High Gain, Typ. 23.9 dB
- High OIP3, Typ. +24.8 dBm
- Low Noise Figure, Typ. 1.8 dB
- Self-Biased from +5 V Supply at 73 mA
- Low Power Consumption, 365 mW

FUNCTIONAL DIAGRAM



SEE ORDERING INFORMATION ON THE LAST PAGE

APPLICATIONS

- Backhaul Radio System
- Satellite Communication
- Test & Measurement Equipment
- Radar, EW, and ECM Defense Systems

PRODUCT OVERVIEW

Mini-Circuits' PMA4-8243LN-D+ is a pHEMT-based low-noise MMIC amplifier with high gain and low power consumption. Operating from 8 to 24 GHz, this amplifier features typical 1.8 dB noise figure, 23.9 dB gain, +12.5 dBm P1dB, and +24.8 dBm OIP3. This device is self-biased, requiring a +5 V supply voltage, and is well-matched to 50Ω for easy integration into dense circuit board layouts.

KEY FEATURES

Features	Advantages
Low Noise Figure, Typ. 1.8 dB	A 50Ω matched low noise MMIC device enables low system noise figure performance which provides minimal signal-to-noise degradation and without the need for complicated discrete-based solutions.
Low Power Consumption, Typ. +5 V at 73 mA	At only 73 mA, this amplifier is ideal for applications with limited available power or densely packed applications where thermal and power management are critical. Additionally, this model only requires a +5 V supply voltage, eliminating the need for complicated sequencing schemes to accommodate multiple voltages.
High OIP3, Typ. +24.8 dBm at 15 GHz	The combination of low noise figure and high OIP3 makes this amplifier ideal for use in sensitive low noise receiver front ends.
Unpackaged Die	Enables integration into hybrid chip and wire assemblies

REV. OR
ECO-027809
PMA4-8243LN-D+
MCL NY
251201

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ELECTRICAL SPECIFICATIONS[1] AT +25°C, V_D = +5 V and Z_0 = 50Ω, UNLESS NOTED OTHERWISE

Parameter	Condition (GHz)	Min.	Typ.	Max.	Units
Frequency Range		8		24	GHz
Gain	8		24.2		dB
	10		23.2		
	15		23.9		
	20		24.7		
	24		25.4		
Input Return Loss	8		15		dB
	10		12		
	15		12		
	20		18		
	24		17		
Output Return Loss	8		10		dB
	10		11		
	15		15		
	20		18		
	24		19		
Isolation	8 - 24		63		dB
Output Power at 1 dB Compression (P1dB)	8		+11.5		dBm
	10		+12.0		
	15		+12.5		
	20		+13.7		
	24		+12.3		
Output Power at Saturation (P_{SAT})[2]	8		+12.4		dBm
	10		+14.3		
	15		+15.8		
	20		+15.8		
	24		+16.3		
Output Third-Order Intercept (OIP3) (P_{OUT} = -5 dBm/Tone)	8		+22.8		dBm
	10		+24.0		
	15		+24.8		
	20		+24.4		
	24		+23.1		
Noise Figure	8		1.7		dB
	10		1.6		
	15		1.8		
	20		1.8		
	24		1.9		
Device Operating Voltage ($V_{D)}$[3]		+4.0	+5.0		V
Device Operating Current (I_{D1})[4]			15.0		mA
Device Operating Current (I_{D2})[4]			20.5		mA
Device Operating Current (I_{D3}+1_{D3b})[4]			37.3		mA
Device Current Variation vs. Temperature[5]			-19.38		µA/°C
Device Current Variation vs. Voltage[6]			0.021		mA/mV

1. Tested on Mini-Circuits Characterization Die Test board. See Figure 3. Characterization performed with direct GSG probe to the RF input and output.
2. Defined as Output Power at which change is 0.1 dB per 1 dB change in input power.
3. $V_D = V_{D1} = V_{D2} = V_{D3}+V_{D3b}$
4. Total Current at P_{IN} = -25 dBm. Total current (I_{D1} + I_{D2} + (I_{D3}+I_{D3b})) increases to 81 mA at P1dB when V_D = +5 V.
5. Tested in Mini-Circuits Characterization Test Board TB-PMA48243LNC+. (Total Current at +105°C – Total Current at -55°C) / (+105°C - -55°C)
6. (Total Current at +5.0 V – Total Current at +4.0 V) / (+5.0 V - +4.0 V)

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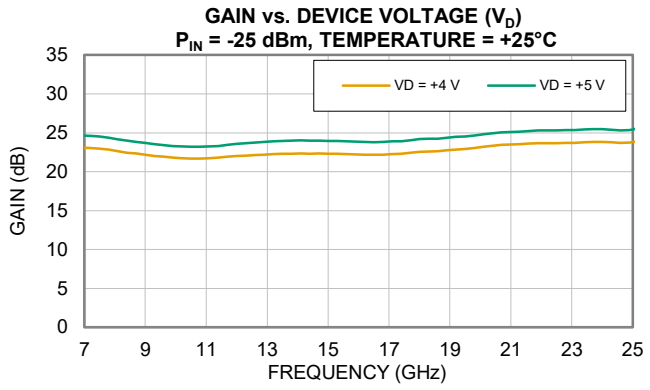
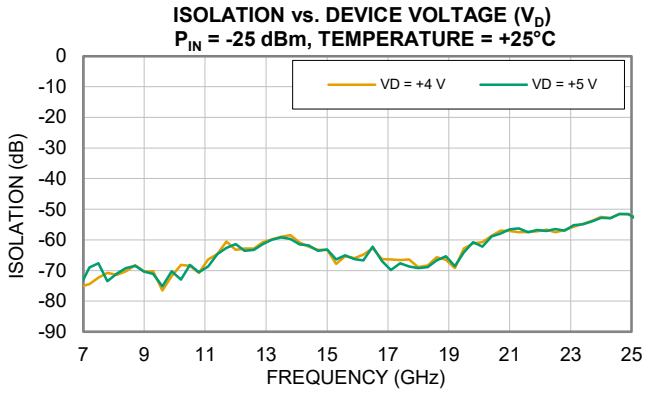
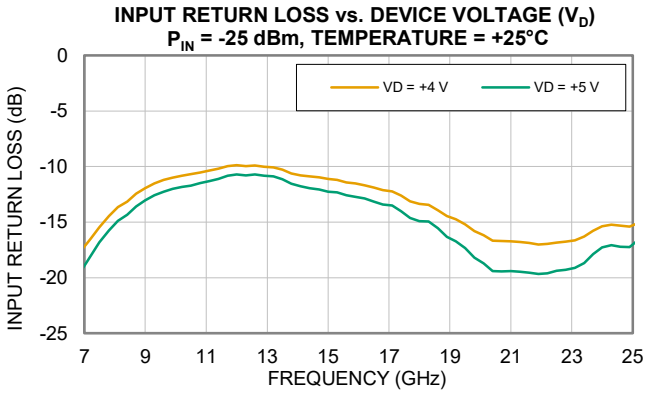
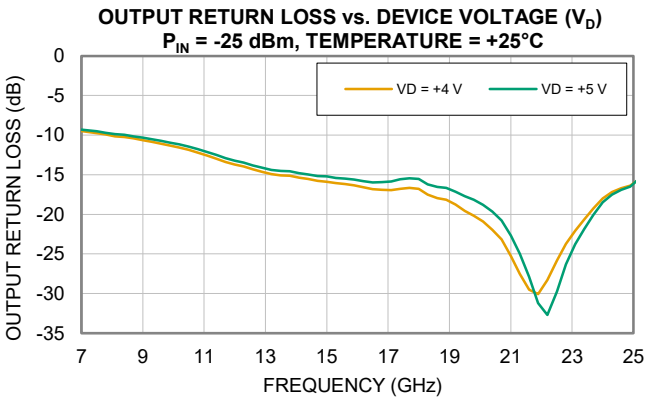
TYPICAL PERFORMANCE GRAPHS

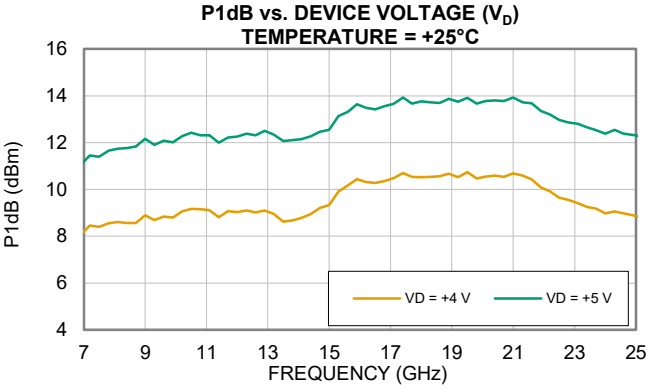
Note: The following data was taken on the Mini-Circuits Die Characterization 8-24 GHz test board (Figure 3).

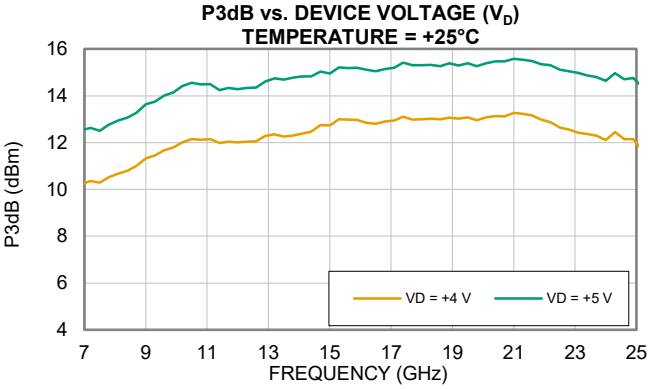












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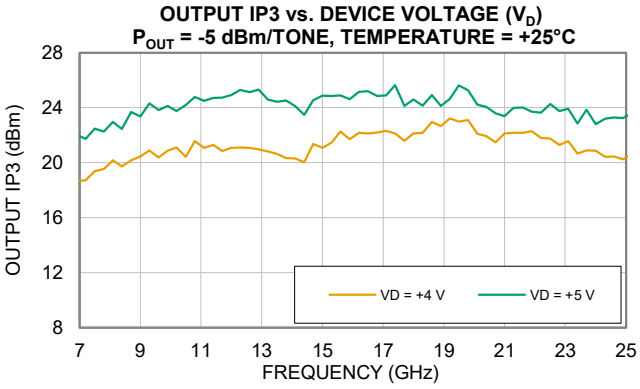

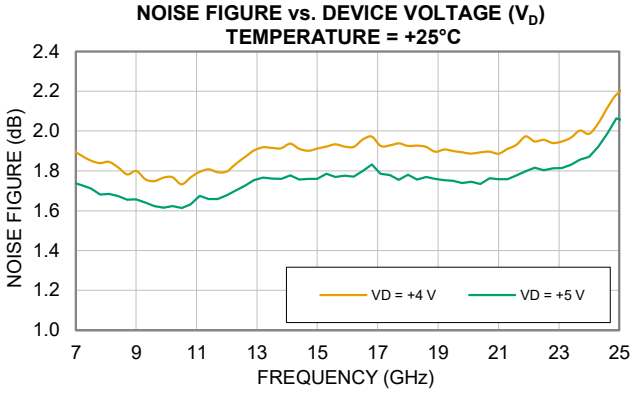

ABSOLUTE MAXIMUM RATINGS[7]

Parameter	Ratings
Operating Temperature[8]	-55°C to +105°C
Storage Temperature[9]	-65°C to +150°C
Junction Temperature[10]	+150°C
Total Power Dissipation	0.66 W
Input Power (CW), V_D = +5 V	+24 dBm
DC Voltage on RF-OUT	+7.3 V
DC Voltage on RF-IN	+2.4 V
DC Drain Voltage on V_D[11]	+13.8 V
DC Drain Current I_{D1}	106 mA
DC Drain Current I_{D2}	102 mA
DC Drain Current I_{D3}+I_{D3b}	97 mA

7. Permanent damage may occur if any of these limits are exceeded. Maximum ratings are not intended for continuous normal operation.
8. Bottom of Die.
9. For die shipped in Gel-Pak see ENV80 (limited by packaging).
10. Peak temperature on top of die.
11. $V_D = V_{D1} = V_{D2} = V_{D3}+V_{D3b}$

THERMAL RESISTANCE

Parameter	Ratings
Thermal Resistance (Θ_{JC})[12]	67.7°C/W

12. Θ_{JC}= (Hot Spot Temperature on Die - Temperature at Ground Lead)/Dissipated Power

ESD RATING[13]

	Class	Voltage Range	Reference Standard
HBM	1B	500 V to < 750 V	ANSI/ESDA/JEDEC JS-001-2023
CDM	C2b	750 to < 1000 V	ANSI/ESDA/JEDEC JS-002-2022

ESD HANDLING PRECAUTION: This device is designed to be Class 1B for HBM. Static charges may easily produce potentials higher than this with improper handling and can discharge into DUT and damage it. As a preventive measure Industry standard ESD handling precautions should be used at all times to protect the device from ESD damage.

13. Tested in 4x4 mm 24-Lead QFN-Style Package

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FUNCTIONAL DIAGRAM

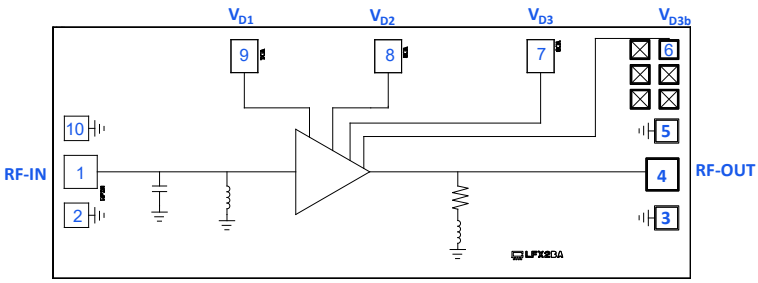

Figure 1. PMA4-8243LN-D+ Functional Diagram

PAD DESCRIPTION

Function	Pad Number	Application Description (Refer to Figure 1)
RF-IN	1	RF-IN Pad connects to RF-Input Port.
RF-OUT	4	RF-OUT Pad connects to RF-Output Port.
V_{D1}	9	DC Input Pad connects to drain input Port, V_{D1}.
V_{D2}	8	DC Input Pad connects to drain input Port, V_{D2}.
V_{D3}	7	DC Input Pad connects to drain input Port, V_{D3}.
V_{D3b}	6	DC Input Pad connects to drain input Port, V_{D3b}.
GND	2, 3, 5, 10 Bottom of Die	Connects to ground. Ground vias connected to the bottom of the die. Bond wires are optional.

DIE OUTLINE: inches [mm], Typical

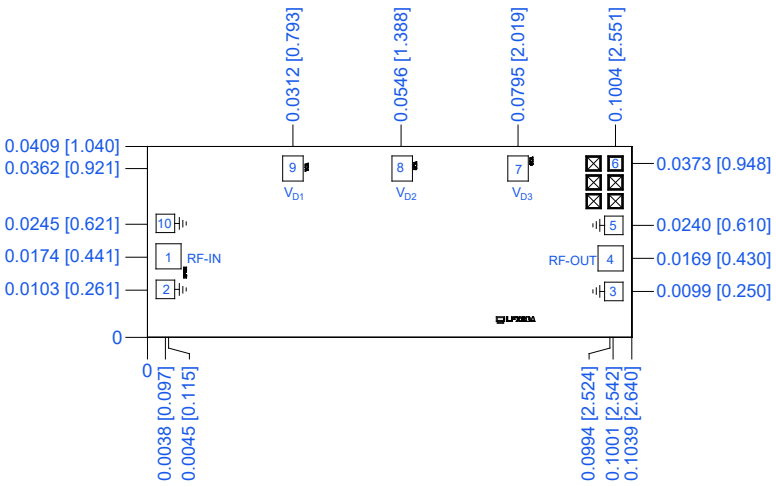

Figure 2. PMA4-8243LN-D+ Die Outline

DIMENSIONS: inches [mm], Typical

Die Size	0.1039 x 0.0409 [2.640 x 1.040]
Die Thickness	0.0039 [0.100]
Bond Pad Sizes:	
Pads 1, 4	0.0049 x 0.0049 [0.125 x 0.125]
Pads 2, 3, 5, 10	0.0035 x 0.0035 [0.090 x 0.090]
Pads 7, 8, 9	0.0039 x 0.0049 [0.100 x 0.125]
Pad 6	0.0028 x 0.0028 [0.070 x 0.070]
Plating (Pads & Bottom of Die)	Gold

CHARACTERIZATION AND APPLICATION CIRCUIT

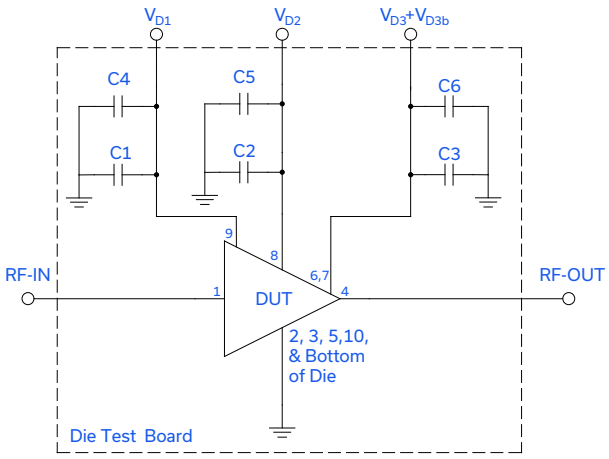

Figure 3. PMA4-8243LN-D+ Characterization and Application Circuit

Electrical Parameters and Conditions
Gain, Return Loss, Output Power at 1dB Compression (P1dB), Output IP3 (OIP3), Saturated Output Power (P_{SAT}), and Noise Figure measured using N5247B PNA-X Microwave Network Analyzer.

Conditions:
1. Gain and Return Loss: P_{IN} = -25 dBm
2. Output IP3 (OIP3): Two tones, spaced 1 MHz apart, -5 dBm/Tone at output.

Power ON/Power OFF Sequence:
PMA4-8243LN-D+ is not sensitive to power ON/OFF sequence. V_{D1}, V_{D2}, and V_{D3}+V_{D3b} can be applied in any order. All three voltage lines may be tied together and applied simultaneously.

Component	Value	Size	Part Number	Manufacturer
C1, C2, C3	100 pF	0402	GRM1555C1H101JA01D	Murata
C4, C5, C6	0.1 µF	0603	GCM188R71E104JA57D	Murata

ASSEMBLY DIAGRAM

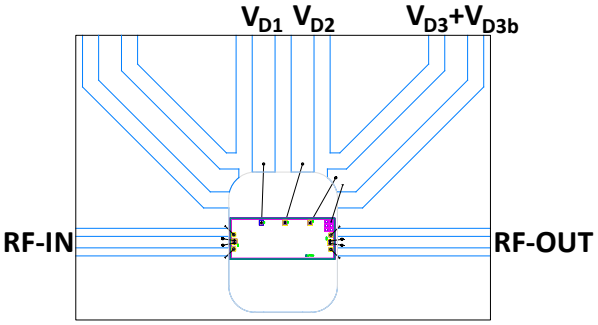

Figure 4. PMA4-8243LN-D+ Assembly Diagram

Refer to the table in Figure 3. for more details on the passive components

- Bond wire diameter: 1 mil
- Bond wire lengths from Die Pad to PCB at RF-IN & RF-OUT ports: 20 mils ± 2 mils
- Typical Gap from Die Edge to PCB Edge: 3 mils
- PCB thickness and material: 10 mils Rogers RO4350B (Thickness: 1 oz copper on each side).

ASSEMBLY AND HANDLING PROCEDURE

1. Storage
   Die should be stored in a dry nitrogen purged desiccator or equivalent.
2. ESD Precautions
   MMIC pHEMT amplifier die are susceptible to electrostatic and mechanical damage. Die are supplied in anti-static protected material, which should be opened only in clean room conditions at an appropriately grounded anti-static workstation.
3. Die Handling and Attachment
   Devices require careful handling using tools appropriate for manipulating semiconductor chips. It is recommended to handle the chips along the edges with a custom designed collet. The die mounting surface must be clean and flat. Using conductive silver-filled epoxy, apply sufficient adhesive to meet the required bond line thickness, fillet height and coverage around the total periphery of the device. The recommended epoxy is Unimec H9890-6A or equivalent. Parts should be cured in a nitrogen-filled atmosphere per manufacturer's recommended cure profile.
4. Wire Bonding
   Openings in the surface passivation above the gold bond pads are provided to allow wire bonding to the die. Thermosonic bonding is recommended with minimized ultrasonic content. Bond force, time, ultrasonic power and temperature are all critical parameters. The suggested interconnect is pure gold, 1 mil diameter wire. Bonds are recommended to be made from the bond pads on the die to the package or substrate. All bond wire length and bond wire height should be kept as short as possible, unless specified by design, to minimize performance degradation due to undesirable series inductance.

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ADDITIONAL DETAILED INFORMATION IS AVAILABLE ON OUR DASHBOARD CLICK HERE

Performance Data & Graphs	Data Graphs S-Parameter (S2P Files) Data Set (.zip file)	
Case Style	Die	
RoHS Status	Compliant	
Die Ordering and Packaging Information	Quantity, Package	Model No.
	Gel - Pak: 5, 10, 50, 100 KGD*	PMA4-8243LN-DG+
	Medium†, Partial wafer: KGD*<703	PMA4-8243LN-DP+
	Full wafer†	PMA4-8243LN-DF+
	†Available upon request contact sales representative. Refer to AN-60-067	
Die Marking	LFX2BA	
Environmental Ratings	ENV80	

* Known Good Die ("KGD") means that the die in question have been subjected to Mini-Circuits DC test performance criteria and measurement instructions and that the parametric data of such die fall within a predefined range. While DC testing is not definitive, it does provide a high degree of confidence that die are capable of meeting typical RF electrical parameters specified by Mini-Circuits.

Notes

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