MMIC DIE

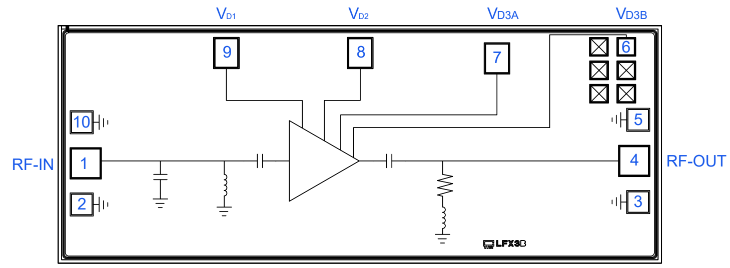
Low Noise Amplifier PMA4-6263LN-D+

50Ω 6 to 26.5 GHz Wideband Amplifier

THE BIG DEAL

- High Gain, Typ. 23.4 dB
- High OIP3, Typ. +23.3 dBm
- Low Noise Figure, Typ. 2.1 dB
- Self-Biased with Low Power Consumption, +4 V @ 55 mA

FUNCTIONAL DIAGRAM



SEE ORDERING INFORMATION ON THE LAST PAGE

APPLICATIONS

- Back Haul Radio Systems
- Satellite Communications
- Test & Measurement Equipment
- Radar, EW, and ECM Defense Systems

PRODUCT OVERVIEW

Mini-Circuits' PMA4-6263LN-D+ is a GaAs pHEMT-based low-noise MMIC amplifier with high gain and low power consumption. Operating from 6 to 26.5 GHz, this amplifier features typical 2.1 dB noise figure, 23.4 dB gain, +12 dBm P1dB, and +23.3 dBm OIP3. This device is self-biased, requiring only a single +4 V supply voltage, is well-matched to 50Ω, and the die measures only 2.64 x 1.04 mm.

KEY FEATURES

Features	Advantages
Low Noise Figure, Typ. 2.1 dB at 20 GHz	This low noise MMIC device enables low system noise figure performance without the need for complicated discrete-based solutions.
Low Power Consumption, Typ. +4 V @ 55 mA	At only 55 mA, this amplifier is ideal for applications with limited available power or densely packed applications where thermal and power management is critical. Additionally, this model only requires a +4 V supply voltage, eliminating the need for complicated sequencing schemes to accommodate multiple voltages.
Unpackaged Die	Suitable for chip and wire hybrid assemblies.

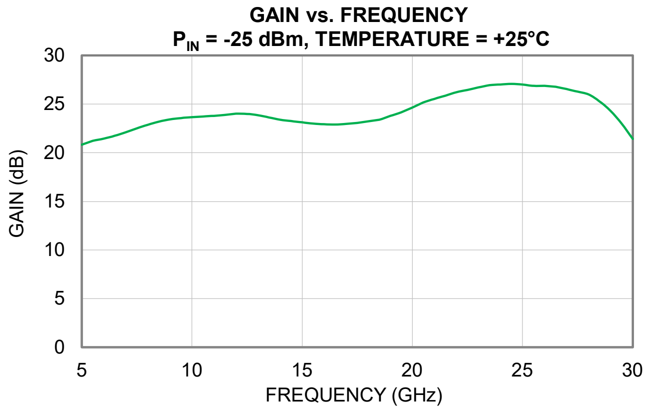
ELECTRICAL SPECIFICATIONS[1] AT +25°C, V_{DD} = +4 V and Z_O = 50Ω, UNLESS NOTED OTHERWISE

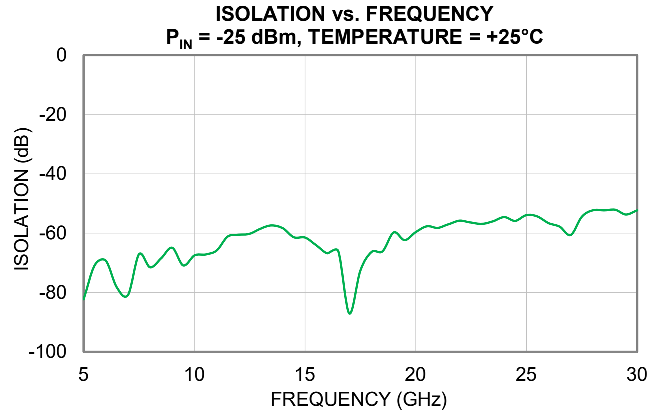
Parameter	Condition (GHz)	Min.	Typ.	Max.	Units
Frequency Range		6		26.5	GHz
Gain	6		21.8		dB
	10		24.0		
	15		23.4		
	20		24.9		
	26.5		27.1		
Input Return Loss	6		10		dB
	10		12		
	15		9		
	20		13		
	26.5		16		
Output Return Loss	6		10		dB
	10		10		
	15		10		
	20		9		
	26.5		10		
Isolation	6 - 26.5		63.1		dB
Noise Figure	6		2.4		dB
	10		1.9		
	15		2.1		
	20		2.1		
	26.5		2.2		
Output Power at 1 dB Compression (P1dB)	6		+10.4		dBm
	10		+10.8		
	15		+12.0		
	20		+12.2		
	26.5		+10.2		
Output Power at Saturation (P_{SAT})[2]	6		+12.4		dBm
	10		+15.2		
	15		+15.5		
	20		+15.7		
	26.5		+15.5		
Output Third-Order Intercept (OIP3) (P_{OUT} = -5 dBm/Tone)	6		+19.6		dBm
	10		+22.6		
	15		+23.3		
	20		+23.9		
	26.5		+22.7		
Device Operating Voltage (V_{DD})[3]		+3.5	+4.0	+5.0	V
Device Operating Current (I_{D1})[4]			10.4		mA
Device Operating Current (I_{D2})[4]			12.9		mA
Device Operating Current (I_{D3})[4,5]			31.8		mA
Device Current Variation vs. Temperature[6]			-45.28		µA/°C
Device Current Variation vs. Voltage[7]			18.0		µA/mV

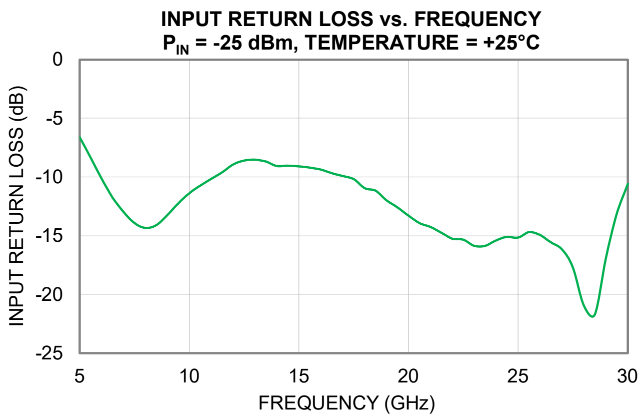
1. Tested on Mini-Circuits Characterization Die Test board. See Figure 3. Loss de-embedded to the RF input and output wire bonds of the device.
2. Defined as Output Power at which change is 0.1 dB per 1 dB change in input power.
3. $V_{DD} = V_{D1} = V_{D2} = V_{D3A}$ & V_{D3B}
4. Current at P_{IN} = -25 dBm. Total current ($I_{D1} + I_{D2} + I_{D3}$) increases to 65 mA at P1dB when V_{DD} = +4 V.
5. $I_{D3} = I_{D3A} + I_{D3B}$
6. (Current at +105°C - Current at -45°C)/(+105°C - -45°C)
7. (Current at +5 V - Current at +3.5 V)/(+5 V - +3.5 V)

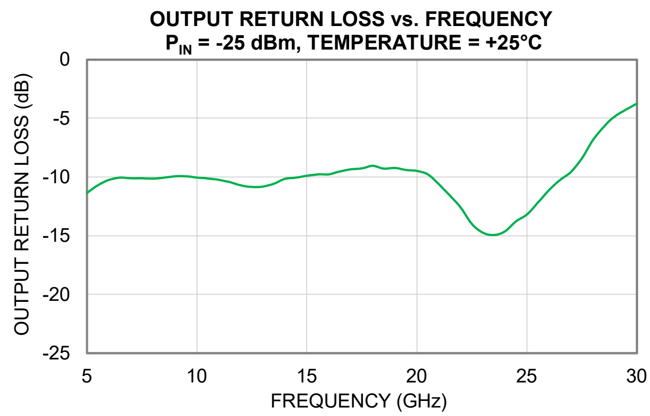
TYPICAL PERFORMANCE GRAPHS

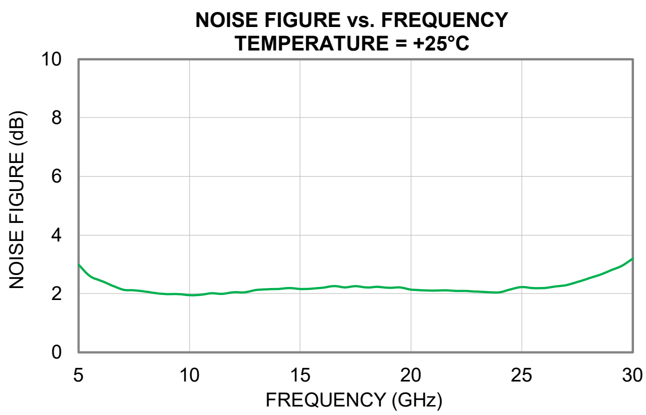
Note: All data taken at nominal condition V_{DD} = +4 V unless noted otherwise. For over voltage and temperature data, see PMA4-6263LN+.

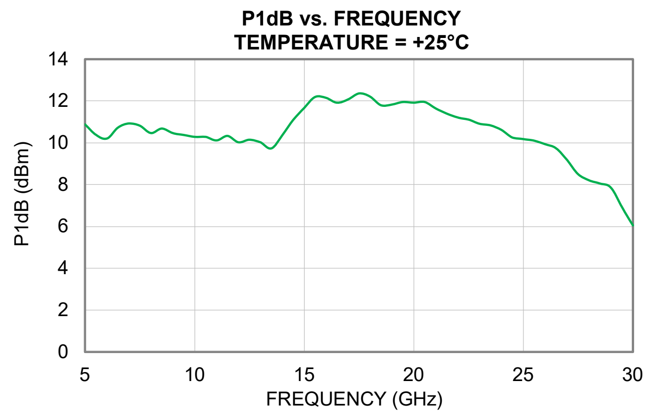












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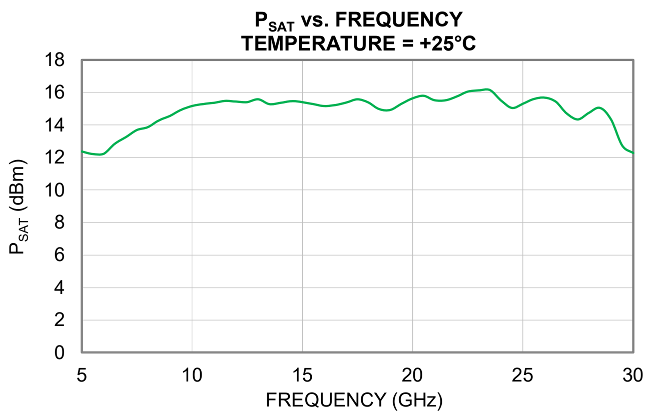

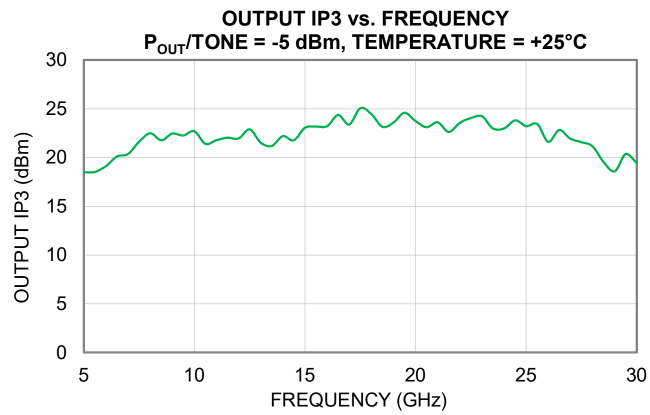

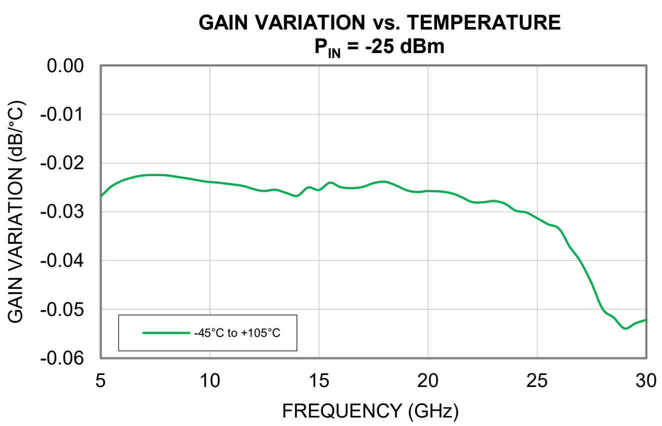

Note: Tested in a 4x4mm 24-lead QFN-style package.

ABSOLUTE MAXIMUM RATINGS[8]

Parameter	Ratings
Operating Temperature[9]	-45°C to +105°C
Storage Temperature[10]	-65°C to +150°C
Total Power Dissipation	0.86 W
Junction Temperature[11]	+175°C
Input Power (CW), V_{DD}[12] = +4 V	+19 dBm
DC Voltage on RF-OUT	+11 V
DC Voltage on RF-IN	+2.6 V
DC Drain Voltage on V_{DD}[12]	+9 V
DC Drain Current I_{D1}	100 mA
DC Drain Current I_{D2}	100 mA
DC Drain Current I_{D3}[13]	90 mA

8. Permanent damage may occur if any of these limits are exceeded. Maximum ratings are not intended for continuous normal operation.
9. Bottom of die.
10. For die shipped in Gel-Pak see ENV80 (limited by packaging).
11. Peak temperature on top of die.
12. $V_{DD} = V_{D1} = V_{D2} = V_{D3A}$ & V_{D3B}
13. $I_{D3} = I_{D3A} + I_{D3B}$

THERMAL RESISTANCE

Parameter	Ratings
Thermal Resistance (Θ_{JC})[14]	52.2°C/W

14. Θ_{JC}= (Hot Spot Temperature on Die - Temperature at Ground Lead)/Dissipated Power

ESD RATING[15]

	Class	Voltage Range	Reference Standard
HBM	1B	500 to < 1000 V	ANSI/ESDA/JEDEC JS-001-2023
CDM	C2A	500 to < 750 V	ANSI/ESDA/JEDEC JS-002-2022

ESD HANDLING PRECAUTION: This device is designed to be Class 1B for HBM. Static charges may easily produce potentials higher than this with improper handling and can discharge into DUT and damage it. As a preventive measure Industry standard ESD handling precautions should be used at all times to protect the device from ESD damage.

15. Tested in 4x4 mm 24-Lead QFN-Style Package

FUNCTIONAL DIAGRAM

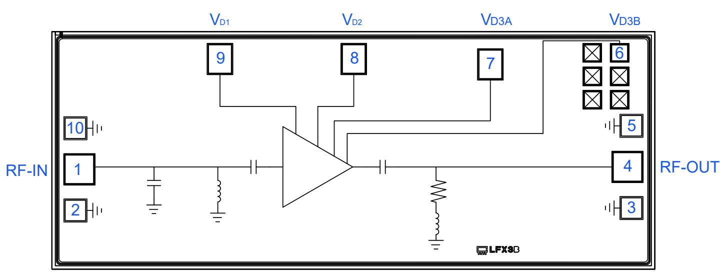

Figure 1. PMA4-6263LN-D+ Functional Diagram

PAD DESCRIPTION

Function	Pad Number	Description (Refer to Figure 3)
RF-IN	1	RF-IN Pad connects to RF Input port.
RF-OUT	4	RF-OUT Pad connects to RF Output port.
V_{D1}	9	DC Input Pad connects to drain input port, V_{D1}.
V_{D2}	8	DC Input Pad connects to drain input port, V_{D2}.
V_{D3A}	7	DC Input Pad connects to drain input port, V_{D3A}.
V_{D3B}	6	DC Input Pad connects to drain input pad, V_{D3B}.
GND	2, 3, 5, 10, & Bottom of Die	Connects to ground. Ground vias connected to the bottom of the die. Bond wires are optional.

DIE OUTLINE: inches [mm], Typical

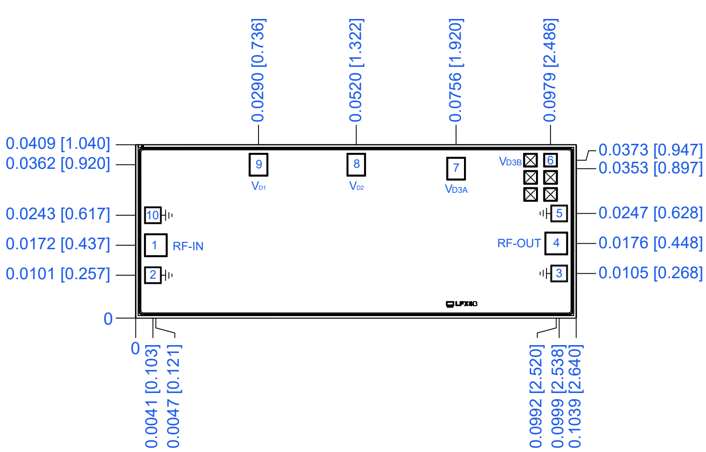

Figure 2. PMA4-6263LN-D+ Outline Drawing.

DIMENSIONS: inches [mm], Typical

Die Size	0.1039 x 0.0409 [2.640 x 1.040]
Die Thickness	0.0040 [0.100]
Bond Pad Sizes:	
Pads 1, 4	0.0049 x 0.0049 [0.125 x 0.125]
Pads 2, 3, 5, 10	0.0035 x 0.0035 [0.090 x 0.090]
Pads 7, 8, 9	0.0039 x 0.0049 [0.100 x 0.125]
Pad 6	0.0028 x 0.0028 [0.070 x 0.070]
Plating (Pads & Bottom of Die)	Gold

EVALUATION BOARD

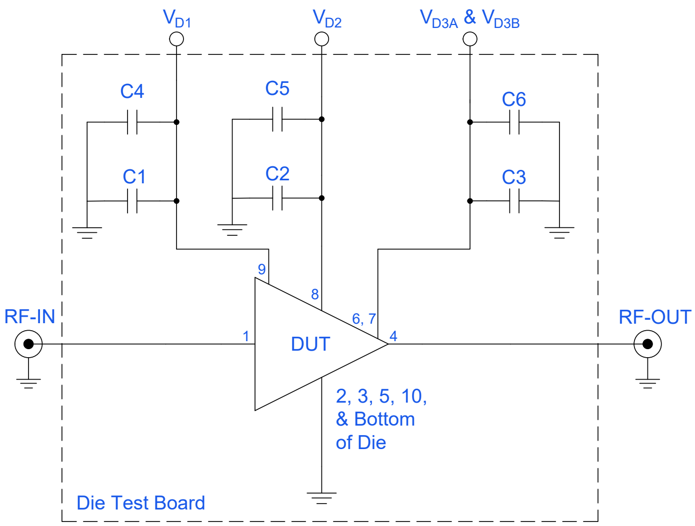

Figure 3. PMA4-6263LN-D+ Characterization and Application Circuit

Electrical Parameters and Conditions
Gain, Return Loss, Output Power at 1dB Compression (P1dB), Output IP3 (OIP3), Saturated Output Power (P_{SAT}), and Noise Figure measured using N5247B PNA-X Microwave Network Analyzer.

Conditions:
1. Gain and Return Loss: P_{IN} = -25 dBm
2. Output IP3 (OIP3): Two tones, spaced 1 MHz apart, -5 dBm/Tone at output.

Power ON/Power OFF Sequence:
PMA4-6263LN-D+ is not sensitive to power ON/OFF sequence. V_{D1}, V_{D2}, and V_{D3A} & V_{D3B} can be applied in any order. All three voltage lines may be tied together and applied simultaneously.

Component	Value	Size	Part Number	Manufacturer
C1, C2, C3	100 pF	0402	GRM1555C1H101JA01D	Murata
C4, C5, C6	0.1 µF	0603	GCM188R71E104JA57D	Murata

ASSEMBLY DIAGRAM

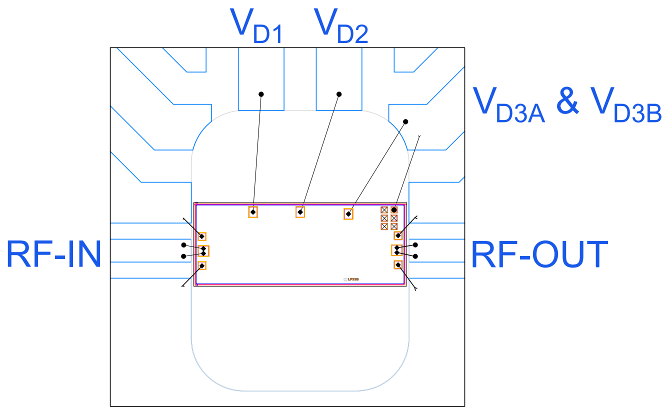

Figure 4. PMA4-6263LN-D+ Assembly Diagram

- Bond wire diameter: 1 mil
- Bond wire lengths from die pad to PCB at RF-IN & RF-OUT ports: 20 mils ± 2 mils
- Bond wire lengths from die pad to V_{D1} port: 41 mils ± 2 mils
- Bond wire lengths from die pad to V_{D2} port: 42 mils ± 2 mils
- Bond wire lengths from die pad to V_{D3A} port: 46 mils ± 2 mils
- Bond wire lengths from die pad to V_{D3B} port: 40 mils ± 2 mils
- Typical gap from die edge to PCB edge: 3 mils
- PCB thickness and material: 10 mils Roger RO4350B (Thickness: 1 oz copper on each side). Die is mounted in the pocket on the brass plate.

ASSEMBLY AND HANDLING PROCEDURE

1. Storage
Die should be stored in a dry nitrogen purged desiccator or equivalent.
2.  ESD Precautions
MMIC pHEMT amplifier die are susceptible to electrostatic and mechanical damage. Die are supplied in anti-static protected material, which should be opened only in clean room conditions at an appropriately grounded anti-static workstation.
3. Die Handling and Attachment
Devices require careful handling using tools appropriate for manipulating semiconductor chips. It is recommended to handle the chips along the edges with a custom designed collet. The die mounting surface must be clean and flat. Using conductive silver-filled epoxy, apply sufficient adhesive to meet the required bond line thickness, fillet height and coverage around the total periphery of the device. The recommended epoxy is Ablestik 84-1 LMISR4 or equivalent. Parts should be cured in a nitrogen-filled atmosphere per manufacturer's recommended cure profile.
4. Wire Bonding
Openings in the surface passivation above the gold bond pads are provided to allow wire bonding to the die. Thermosonic bonding is recommended with minimized ultrasonic content. Bond force, time, ultrasonic power and temperature are all critical parameters. The suggested interconnect is pure gold, 1 mil diameter wire. Bonds are recommended to be made from the bond pads on the die to the package or substrate. All bond wire length and bond wire height should be kept as short as possible, unless specified by design, to minimize performance degradation due to undesirable series inductance.

ADDITIONAL DETAILED INFORMATION IS AVAILABLE ON OUR DASHBOARD CLICK HERE

Performance Data & Graphs	Data Graphs S-Parameter (S2P Files) Data Set (.zip file)	
Case Style	Die	
RoHS Status	Compliant	
Die Ordering and Packaging Information	Quantity, Package	Model No.
	Gel - Pak: 5, 10, 50, 100 KGD*	PMA4-6263LN-DG+
	Medium†, Partial wafer: KGD*<703	PMA4-6263LN-DP+
	Full wafer†	PMA4-6263LN-DF+
	†Available upon request contact sales representative. Refer to AN-60-067	
Die Marking	LFX3B	
Environmental Ratings	ENV80	

*Known Good Die ("KGD") means that the die in question have been subjected to Mini-Circuits DC test performance criteria and measurement instructions and that the parametric data of such die fall within a predefined range. While DC testing is not definitive, it does provide a high degree of confidence that die are capable of meeting typical RF electrical parameters specified by Mini-Circuits.