Digital Controlled Variable Gain Amplifier DVGA2-33+

50Ω 0.05 to 3 GHz
31.5 dB, 0.5 dB Step, 6 Bit Serial Control

The Big Deal

- Integrated Amplifier and Digital Attenuator
- 19 dB Gain / 31.5 dB Gain Control
- Flat frequency response, ±0.7 dB (700-2100 MHz)

CASE STYLE: DG1677

Product Overview

The DVGA2-33+ is a 50Ω RF Digital Variable Gain Amplifier that offers an attenuation of 31.5 dB in 0.5 dB steps using a 6-bit serial interface attenuator and 19dB gain using a InGap HBT amplifier. Step attenuator used in DVGA2-33+ is produced using a unique combination of CMOS process on silicon, offering the performance of GaAs, with the advantages of conventional CMOS devices.

Key Features

Feature	Advantages
31.5 dB attenuation in 0.5 dB step size	Combining medium gain and a wide range of gain control makes the DVGA2-33+ an ideal building block for any RF chain where level setting control is required in a small space.
Flat frequency response, ±0.7 over 700-2100 MHz	No need for external components to flatten gain.
Medium Gain, 19 dB	Incorporating multiple stages of amplification, the DVGA2-33+ provides medium gain over a wideband reducing cost and PCB board space.
Good IP3, +30 dBm at 1.0 GHz	Use in receivers and transmitters giving the users advantage in instantenous spur free dynamic range over wide bandwidths.
Output Power, +16.3 dBm at 1.0 GHz	The DVGA2-33+ maintains consistent output power capability over the full attenuation range and operating temperature range making it ideal to be used in remote applications such as LNB's as the L Band driver stage.
Attenuation Step size, 0.5 dB, accuracy 0.1 to 0.5 dB typ. Total attenuation, 31.5 dB	Enables precise control of gain in 0.5 dB steps up to 31.5 dB.
MCLP Package	Low Inductance, repeatable transitions, excellent thermal pad.
PCB area reduction	The DVGA2-33+ combines multiple functions common to TX/RX architectures into a single 5x5mm package
Flexibility in the application block diagram	The DVGA2-33+ provides access to the internal circuit through external jumper (see simplified schematic) enables designers flexibility to incorporate a wide range of additional circuits.

Digital Controlled Variable Gain Amplifier 50Ω 50 - 3000 MHz

19 dB Gain, 0.5 dB Step, 31.5 dB Attenuation, 6 Bit Serial Control

Product Features

- 31.5 dB Gain control 0.5dB step size
- Gain, 19 dB nominal at 0dB attenuation and 1 GHz
- Useable to 4 GHz
- Serial control interface
- Small size 5.0 x 5.0 mm

DVGA2-33+

CASE STYLE: DG1677

+RoHS Compliant

The +Suffix identifies RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications

Typical Applications

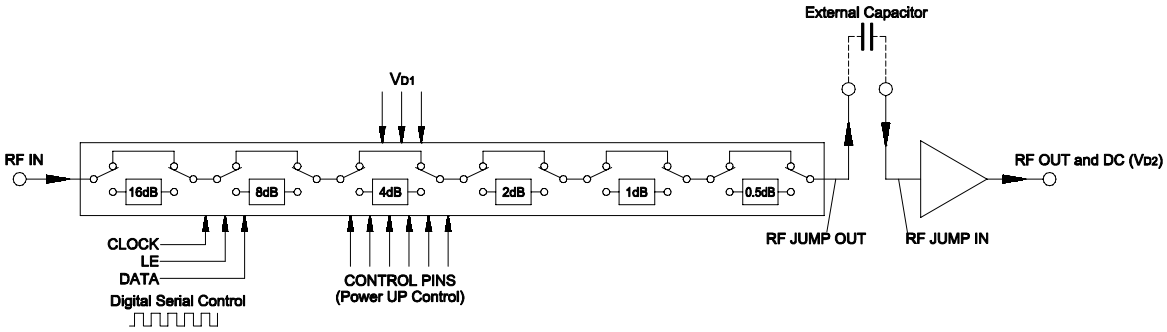
- Base Station Infrastructure
- GPS
- LTE
- WCDMA

General Description

The DVGA2-33+ is a 50Ω RF Digital Variable Gain Amplifier that offers an attenuation of 31.5 dB in 0.5 dB steps using a 6-bit serial interface attenuator and 19dB gain using a InGap HBT amplifier. Step attenuator used in DVGA2-33+ is produced using a unique combination of CMOS process on silicon, offering the performance of GaAs, with the advantages of conventional CMOS devices.

Simplified Schematic

(Refer to Table 1 for Pad description)



Notes

A. Performance and quality attributes and conditions not expressly stated in this specification document are intended to be excluded and do not form a part of this specification document.
B. Electrical specifications and performance data contained in this specification document are based on Mini-Circuit's applicable established test performance criteria and measurement instructions.
C. The parts covered by this specification document are subject to Mini-Circuits standard limited warranty and terms and conditions (collectively, "Standard Terms"); Purchasers of this part are entitled to the rights and benefits contained therein. For a full statement of the Standard Terms and the exclusive rights and remedies thereunder, please visit Mini-Circuits' website at www.minicircuits.com/MCLStore/terms.jsp

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RF Electrical Specifications[1] at 25°C, 50Ω With V_{D1}=+3.0V, V_{D2}=+5V

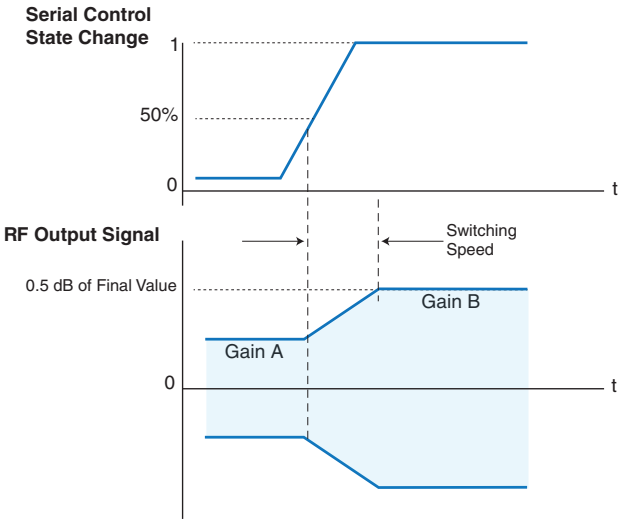
Parameter	Condition (GHz)	Min.	Typ.	Max.	Units
Frequency Range		0.05		3.0	GHz
Gain (at 0 dB attenuation)	0.05 1.0 2.0 3.0	— — 16.3 —	20.3 19.2 18.1 15.5	— — 20.0 —	dB
Input Return Loss (all states)	0.05 1.0 2.0 3.0	— — — —	12.6 13.4 15.7 11.0	— — — —	dB
Output Return Loss (all states)	0.05 1.0 2.0 3.0	— — — —	16.5 13.6 14.5 9.7	— — — —	dB
Output Power @ 1 dB compression (all states)	0.05 1.0 2.0 3.0	— — — —	17.1 16.3 17.5 16.1	— — — —	dBm
Output IP3 (all states)	0.05 1.0 2.0 3.0	— — — —	32.4 29.6 30.6 29.1	— — — —	dBm
Noise Figure (at 0 dB attenuation)	0.05 1.0 2.0 3.0	— — — —	5.0 5.4 5.7 6.4	— — — —	dB
Accuracy @ **0.5 dB** Attenuation Setting	0.05 - 1.0	—	0.04	0.12	dB
	1.0 - 3.0	—	0.09	0.23	
Accuracy @ **1 dB** Attenuation Setting	0.05 - 1.0	—	0.03	0.13	dB
	1.0 - 3.0	—	0.12	0.3	
Accuracy @ **2 dB** Attenuation Setting	0.05 - 1.0	—	0.06	0.16	dB
	1.0 - 3.0	—	0.38	0.6	
Accuracy @ **4 dB** Attenuation Setting	0.05 - 1.0	—	0.05	0.3	dB
	1.0 - 3.0	—	0.42	0.7	
Accuracy @ **8 dB** Attenuation Setting	0.05 - 1.0	—	0.15	0.4	dB
	1.0 - 3.0	—	0.42	0.7	
Accuracy @ **16 dB** Attenuation Setting	0.05 - 1.0	—	0.24	0.6	dB
	1.0 - 3.0	—	0.50	1.1	
Thermal Resistance (Amplifier)[2]		—	91	—	°C/W

1. Measured in Mini-Circuits characterization test board TB-674+. See characterization Test Circuit (Fig. 2)
2. Junction to ground paddle

Attenuation Switching Specifications

Parameter	Min.	Typ.	Max.	Units
Switching Speed, 50% Control to 0.5dB of Attenuation Value	—	1.0	—	µSec
Switching Rep Rate	—	—	25	KHz

Figure 1. Switching Speed



DC Electrical Specifications

Parameter	Min.	Typ.	Max.	Units
Supply Voltage, V_{D1}	2.7	3.0	3.3	V
V_{D2}	4.75	5.0	5.25	V
Supply Current, I_{D1}*	—	—	100*	µA
I_{D2}	—	69	78	mA
Control Input Low**	—	—	0.3xV_{D1}	V
Control Input High**	0.7xV_{D1}	—	—	V
Control Current**	—	—	1	µA

*During turn-on and transition between attenuation states I_{D1} may increase up to 2mA

Absolute Maximum Ratings

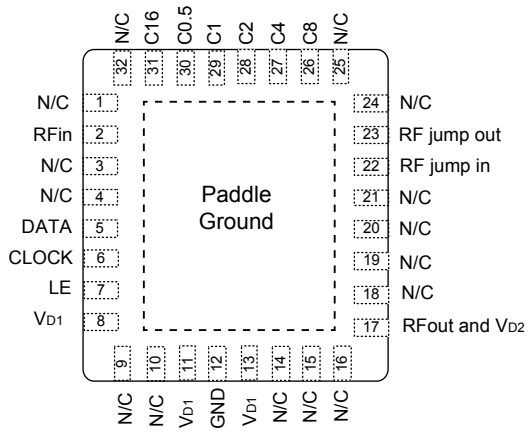
Parameter	Ratings
Operating Temperature (ground pad)	-40°C to 85°C
Storage Temperature	-65°C to 150°C
V_{D1}	-0.3V Min., 4V Max.
V_{D2}	5.7V
Voltage on any control input**	-0.3V Min., V_{D1}+0.3V Max.
Input Power	+13dBm

**Data, clock or latch enable.

Permanent damage may occur if any of these limits are exceeded.

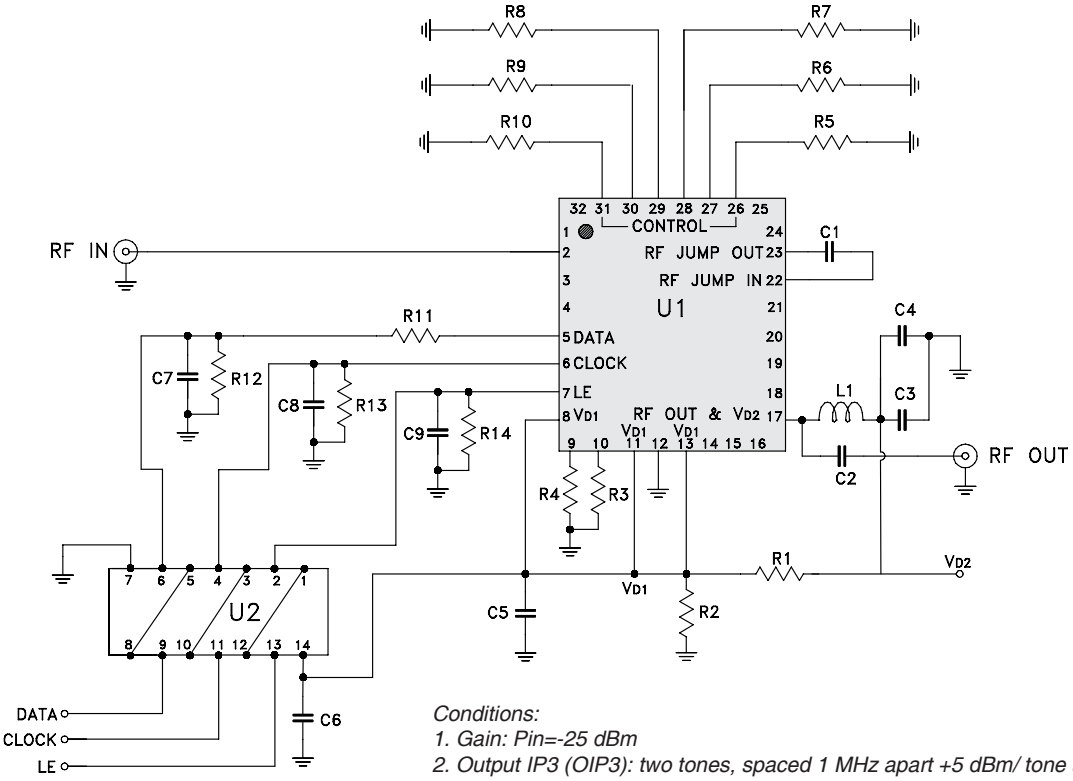
Table 1. Pad Description

Pin Number	Function	Description
1	N/C	Not Connected
2	RF IN	RF Input Port (Note 1)
3	N/C	Not Connected
4	N/C	Not Connected
5	DATA	Serial Interface Data Input (Note 3)
6	CLOCK	Serial Interface Clock Input
7	LE	Latch Enable Input (Note 2)
8	V_{D1}	V_{D1} Power Supply Input (Note 6)
9	N/C	Not Connected (Note 6)
10	N/C	Not Connected
11	V_{D1}	V_{D1} Power Supply Input
12	GND	Ground
13	V_{D1}	V_{D1} Power Supply Input
14	N/C	Not Connected
15	N/C	Not Connected
16	N/C	Not Connected
17	RF OUT &V_{D2}	RF output and V_{D2} on same pad (external Bias Tee) (Note1,6)
18	N/C	Not Connected
19	N/C	Not Connected
20	N/C	Not Connected
21	N/C	Not Connected
22	RF JUMP IN	Interstage RF Jumper Input (Note 1)
23	RF JUMP OUT	Interstage RF Jumper Output (Note 1)
24	N/C	Not Connected
25	N/C	Not Connected
26	C8	Power Up Control for 8dB Att. Bit (Note 4)
27	C4	Power Up Control for 4dB Att. Bit (Note 4)
28	C2	Power Up Control for 2dB Att. Bit (Note 4)
29	C1	Power Up Control for 1dB Att. Bit (Note 4)
30	C0.5	Power Up Control for 0.5dB Att. Bit (Note 4)
31	C16	Power Up Control for 16dB Att. Bit (Note 4)
32	N/C	Not Connected
PADDLE	GND	Ground (Note5)



Notes:
1. All RF input and output ports shall be AC coupled with external blocking capacitor.
2. Latch Enable (LE) has an internal 100KΩ pull-up resistor to V_{D1}
3. Place a 10KΩ resistor in series, as close to pin as possible to avoid freq. resonance (see layout drawing PL-355).
4. Refer to Power-up Control Settings.
5. The exposed solder pad on the bottom of the package (See Pin Configuration) must be grounded for proper device operation
6. See application and characterization test circuit and layout drawing PL-355.

Application and Characterization Test Circuit



Conditions:
1. Gain: Pin=-25 dBm
2. Output IP3 (OIP3): two tones, spaced 1 MHz apart +5 dBm/ tone at output.
3. Schmitt trigger used in characterization circuit. Not required when application circuit includes recommended level settings.

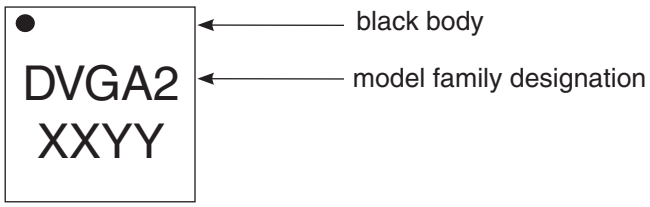
Figure 2. Schematic of Test Circuit used for Characterization. (DUT soldered on Mini-Circuits Characterization Test Board TB-674+). Gain, output power at 1 dB compression (P1dB) Output IP3 (OIP3), Noise Figure are measured using Agilent's N5242A PNA-X Microwave Network Analyzer.

Bill of Materials

Ref. Des.	Value / Description	Case Style, Size
C1	1000pF	0402
C2	1000pF	0805
C3	1µF	0805
C4	100pF	0402
C5, C7, C8, C9	100pF	0603
C6	0.47µF	0805
L1	390nH	0402
R1	475Ω	0603
R2	681Ω	0603
R3 ~ R14	10kΩ	0603
U2	HEX Inverter Trigger Fairchild P/N MM74HC14M	
U1	DVGA2-33+	

Note: To operate down to 10 MHz, change:
1) C1 & C2 to 2400 pF and
2) L1 to 3.9 µH
3) C1, C2, L1 should be free of resonance over usage BW

Product Marking



Simplified Schematic

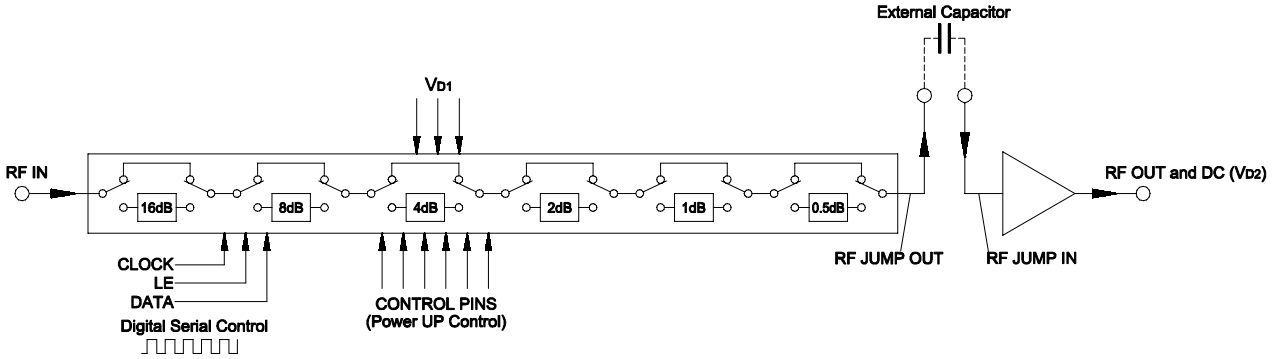


Figure 3. The DVGA2-33+ Serial interface consists of 6 control bits that select the desired attenuation state, as shown in Table 2 Truth Table.

Table 2. Truth Table

Attenuation State	C16	C8	C4	C2	C1	C0.5
Reference	0	0	0	0	0	0
0.5 (dB)	0	0	0	0	0	1
1 (dB)	0	0	0	0	1	0
2 (dB)	0	0	0	1	0	0
4 (dB)	0	0	1	0	0	0
8 (dB)	0	1	0	0	0	0
16 (dB)	1	0	0	0	0	0
31.5 (dB)	1	1	1	1	1	1
Note: Not all 64 possible combinations of C0.5 - C16 are shown in table						

The serial interface is a 6-bit serial in, parallel-out shift register buffered by a transparent latch. It is controlled by three CMOS-compatible signals: Data, Clock, and Latch Enable (LE). The Data and Clock inputs allow data to be serially entered into the shift register, a process that is independent of the state of the LE input. The LE input controls the latch. When LE is HIGH, the latch is transparent and the contents of the serial shift register control the attenuator. When LE is brought LOW, data in the shift register is latched. The shift register should be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input should then be toggled HIGH and brought LOW again, latching the new data. The timing for this operation is defined by Figure 4 (Serial Interface Timing Diagram) and Table 3 (Serial Interface AC Characteristics).

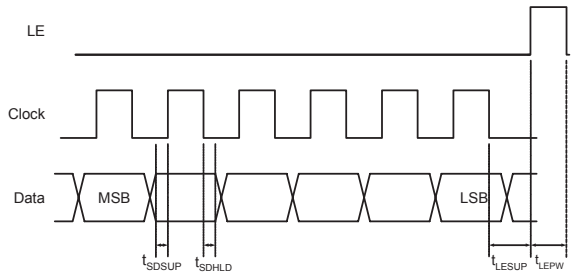


Figure 4. Serial Interface Timing Diagram

Table 3. Serial Interface AC Characteristics (V_{D1}=3V)

Symbol	Parameter	Min.	Max.	Units
f_{clk}	Serial data clock frequency (Note 1)		10	MHz
t_{clkH}	Serial clock HIGH time	30		ns
t_{clkL}	Serial clock LOW time	30		ns
t_{LESUP}	LE set-up time after last clock falling edge	10		ns
t_{LEPW}	LE minimum pulse width	30		ns
t_{SDSUP}	Serial data set-up time before clock rising edge	10		ns
t_{SDHLD}	Serial data hold time after clock falling edge	10		ns

Note 1. fclk verified during the functional pattern test. Serial programming sections of the functional pattern are clocked at 10MHz to verify fclk specification.

The DVGA2-33+, uses a common 6-bit serial, as shown in Table 4: 6-Bit attenuator Serial Programming Register Map. The first bit, the MSB, corresponds to the 16-dB Step and the last bit, the LSB, corresponds to the 0.5dB step.

Table 4. 6-Bit attenuator Serial Programming Register Map

B5	B4	B3	B2	B1	B0
C16	C8	C4	C2	C1	C0.5

MSB (first in) — LSB (last in)

Power-up Control Settings

The DVGA2-33+ always assumes a specifiable attenuation setting on power-up, allowing a known attenuation state to be established before an initial serial control word is provided. When the attenuator powers up, the six control bits are set to whatever data is present on the six control inputs (C0.5 to C16). This allows any one of the 64 attenuation settings to be specified as the power-up state.

Additional Detailed Technical Information *additional information is available on our dash board. To access this information click here*	
Performance Data	Data Table
	Swept Graphs
	S-Parameter (S2P Files) Data Set (.zip file)
Case Style	DG1677 *Plastic package, exposed paddle, lead finish: Ni/Pd/Au*
Tape & Reel **Standard quantities available on reel**	F68 *7" reels with 20,50,100,200, 500 or 1K devices*
Suggested Layout for PCB Design	PL-371
Evaluation Board	TB-674+
Environmental Ratings	ENV66

ESD Rating

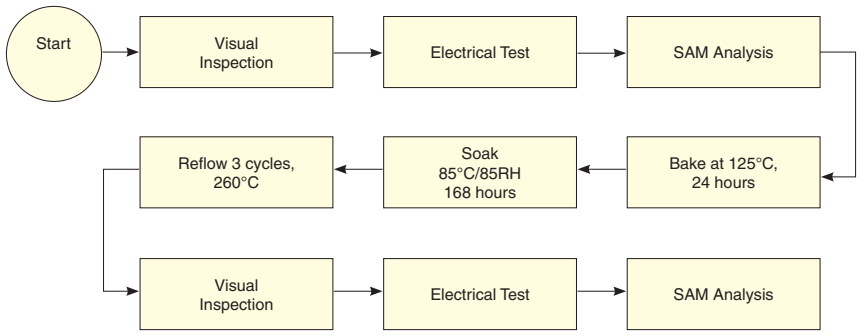
Human Body Model (HBM): Class 1A (250 to <500V) in accordance with ANSI/ESD STM 5.1 - 2001

Machine Model (MM): Class M1 (100V) in accordance with ANSI/ESD STM5.2-1999

MSL Rating

Moisture Sensitivity: MSL1 in accordance with IPC/JEDEC J-STD-020D

MSL Test Flow Chart



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