MMIC DIE

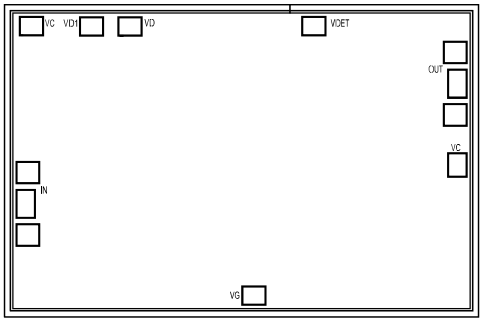
Wideband Amplifier

AVA-054-D+

50Ω DC to 50 GHz

THE BIG DEAL

- Wideband, DC to 50 GHz
- Gain Flatness, ±2.2 dB
- Typical P1dB, +19 dBm



+RoHS Compliant
The +Suffix identifies RoHS Compliance.
See our website for methodologies and qualifications

SEE ORDERING INFORMATION ON THE LAST PAGE

APPLICATIONS

- 5G MIMO and Back Haul Radio Systems
- Satellite Ka-band Communications
- Test and Measurement Equipment
- Radar, EW, and ECM Defense Systems

PRODUCT OVERVIEW

AVA-054-D+ is a GaAs PHEMT MMIC Distributed Amplifier designed for use in microwave and millimeter wave transceiver systems and signal sources operating from 0.05 to 50 GHz. The amplifier provides 16 dB of Gain, +19 dBm P1dB and +26 dBm OIP3 while operating from a +5V supply with 160 mA current consumption. The MMIC Amplifier includes an on chip power detector for power monitoring and the Gain can be varied over a 20 dB range with a control voltage. The AVA-054-D+ performance characteristics and features makes the device useful for a wide range of Test and Measurement Equipment and Defense Systems operating in frequency ranges from 0.05-50 GHz.

KEY FEATURES

Features	Advantages
Wideband: DC to 50 GHz	General purpose wideband amplifier is suitable for various applications.
Gain: 16.5 dB ± 1.5 dB from 0.1 to 45 GHz.	Minimizes the number of gain stages required to achieve published Gain, reducing component count, cost and complexity.
P1dB: +19.5 dBm ± 1.6 dB	Useful as a driver amplifier. Can be used as a final amplifier in local oscillator chains to drive +17 dBm mixers.
On Chip Power Detector	Enables power monitoring and AGC loops.
Adjustable Gain with control voltage	Useful temperature compensation and AGC of wide bandwidth signal chains.
Unpackaged die	Enables user to integrate it directly into hybrids.

REV. A
ECO-021862
AVA-054-D+
MCL NY
240529

ELECTRICAL SPECIFICATIONS[1] AT 25°C, V_C = OPEN, V_{DD} = +5V, Zo = 50Ω, UNLESS NOTED OTHERWISE

Parameter	Condition (GHz)	V_{DD} = +5V, I_{DD} = 160mA			Units
		Min.	Typ.	Max.	
Frequency Range		DC		50	GHz
Gain[2]	0.1		17.3		dB
	10		15.6		
	20		16.1		
	30		17.4		
	40		17.4		
	50		13		
Input Return Loss	0.1		12		dB
	10		15		
	20		17		
	30		22		
	40		12		
	50		25		
Output Return Loss	0.1		27		dB
	10		21		
	20		16		
	30		16		
	40		14		
	50		12		
Reverse Isolation	0.1-50		36		dB
Output Power at 1 dB Compression	0.1		+20.7		dBm
	10		+20.0		
	20		+19.3		
	30		+17.9		
	40		+17.0		
	50		--		
Output Third-Order Intercept (P_{OUT} = +5 dBm/Tone)	0.1		+32		dBm
	10		+27.3		
	20		+26.9		
	30		+22.5		
	40		+20.8		
	50		--		
Noise Figure	0.1		5.5		dB
	10		3.1		
	20		4.0		
	30		5.5		
	40		7.8		
	50		11.8		
Device Operating Voltage (V_{DD})			+5.0		V
Device Operating Current (I_{DD})			160.0		mA
Device Gate Voltage (V_{GG})			-0.76		V
Device Gate Current (I_{GG})			-0.24		µA
Thermal Resistance, Junction-to-Ground Lead (ΘJC)			17.8		°C/W

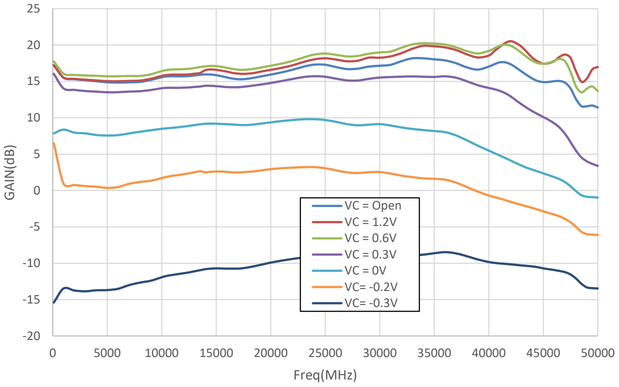
1. Die is soldered and measured on Mini-Circuits die characterization board. See Characterization & Application Circuit (Fig. 2).
2. If V_C is open, the measured voltage is +1.33V.

MAXIMUM RATINGS[3]

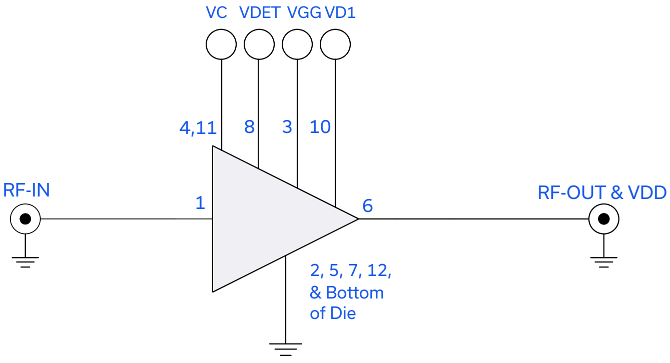
Parameter	Ratings
Operating Temperature	-40°C to +85°C
Junction Temperature	+150°C[4]
Total Power Dissipation	1.8 W
Input Power (CW)	+17dBm
Drain Voltage (V_{DD})	+7.5 V
Gate Voltage (V_{GG})	-1.6 V to -0.5 V
Drain Current (I_{DD})	240 mA
Gate Current (I_{GG})	-5 mA to 0 mA
Control Voltage (V_C)	-1 V to 1.2 V

[3] Permanent damage may occur if these limits are exceeded.
[4] Tj = +85°C + (VDD)*(IDD)*(ΘJC) = +99°C. Keeping Tj below +99°C will ensure MTTF > 100 Years.

FIG 1. GAIN VS. CONTROL VOLTAGE (VC)

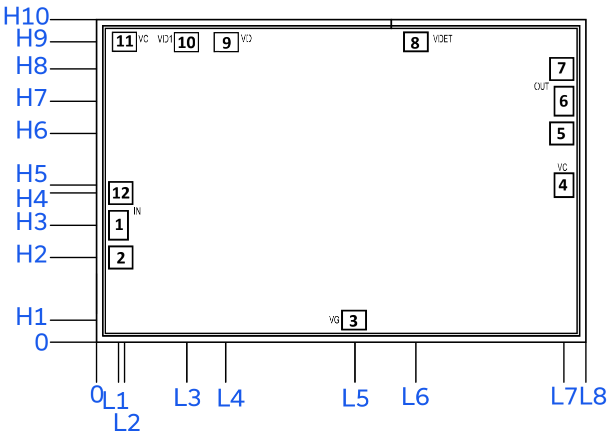


SIMPLIFIED SCHEMATIC AND PAD DESCRIPTION



Function	Pad Number	Description
RF-IN	1	RF Input Pad
VGG	3	Gate Bias Pad
VC	4, 11	Gain Control Pads
RF-OUT & VDD	6	RF Output and Drain Pad
VDET	8	Voltage Detector Pad
VD	9	Alternative Drain Bias Pad, connects to Pad #6 internally.
VD1	10	Alternative Drain Bias Pad. It is terminated by C2
GROUND	2, 5, 7, 12, & Bottom of die	The bond pads are connected to backside through vias and do no require wire-bond connections to ground.

BONDING PAD POSITION



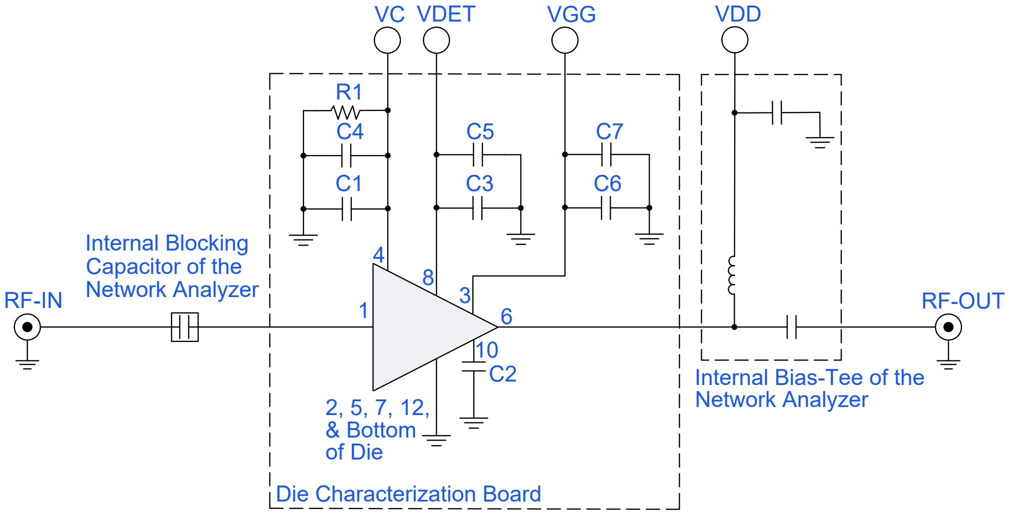
DIMENSIONS IN μm, TYP.

L1	L2	L3	L4	L5	L6	L7	L8
88	112	363	520	1040	1285	1882	1970

H1	H2	H3	H4	H5	H6	H7	H8	H9	H10
89	341	471	601	633	841	971	1101	1211	1300

Thickness	Die size	Pad size 1,6	Pad size 2, 5, 7, 12	Pad size 3, 8, 9, 10, & 11	Pad size 4
100	1970 x 1300	73 x 113	91 x 86	93 x 73	73 x 93

CHARACTERIZATION & APPLICATION CIRCUIT



Component	Size	Value	Part Number	Manufacturer
C1, C3, & C6	100pF	22x22mil	MA4M3100	MACOM Inc.
C2	820pF	20x20mil	SKT02C821M11A6	TECDIA Inc.
C4, C5, & C7	0.1µF	0402	GRM155R71C104KA88D	Murata
R1	200Ω	0603	RK73H1JTTD2001F	KOA

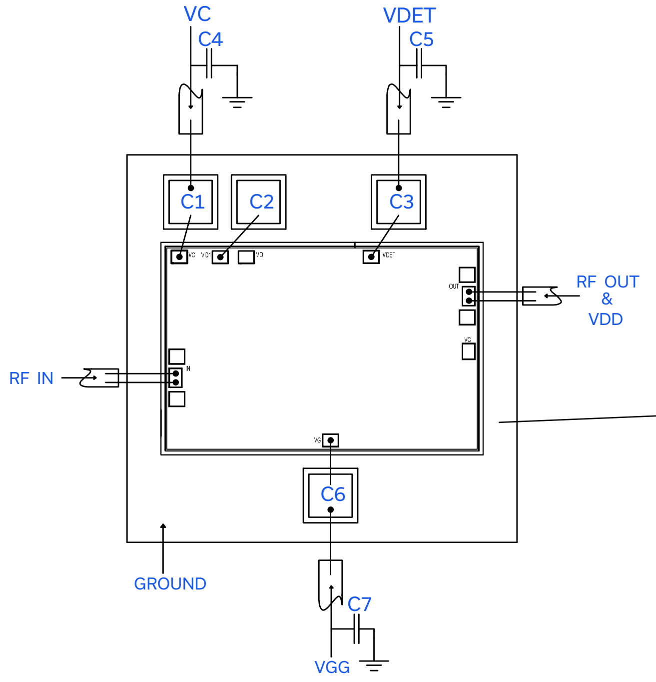
Fig 2. Characterization & Application Circuit
Note: This block diagram is used for characterization (Die is attached and wire-bonded on die characterization test board). Gain, Return Loss, Output Power at 1dB Compression (P1dB), Output IP3 (OIP3) and Noise Figure measured using Agilent's N5245B Microwave Network Analyzer.

Conditions:
1. VDD = +5V,
2. VGG is set to obtain desired IDD as shown in specification table.
3. Gain and Return Loss: Pin= -25 dBm
4. Output IP3 (OIP3): Two Tones, spaced 1 MHz apart, +5 dBm/Tone at output.

Switch ON/OFF sequence:
1. To switch the amplifier ON:
a. Set VGG = -1.2V. Apply VGG.
b. Set VDD = +5V. Apply VDD
c. Adjust VGG to get IDD = 160mA (Typically, VGG = -0.76V)
d. Apply RF Signal.

2. To switch the amplifier OFF:
a. Turn off RF Signal
b. Adjust VGG down to -1.2V.
c. Turn off VDD.
d. Turn off VGG

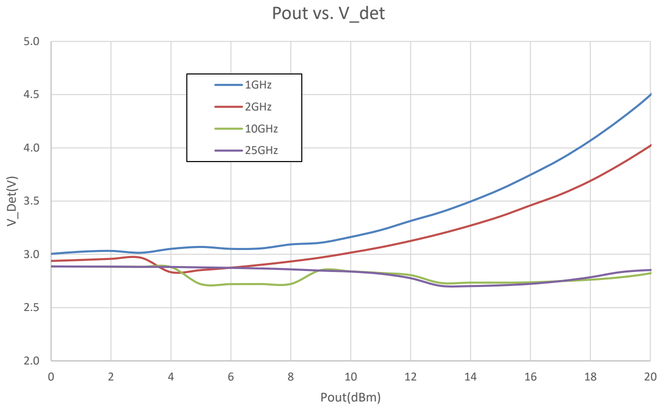
ASSEMBLY DRAWING



Note: Tested on die characterization board with following bond lengths:
1. Typical bond length for RF-IN: 360μm (14mils)
2. Typical bond length for RF-OUT & VDD: 360μm (14mils)
3. Typical bond lengths from die, capacitors, VGG, VDET, and VC were kept as short as possible.
4.Components list given in Figure 2.

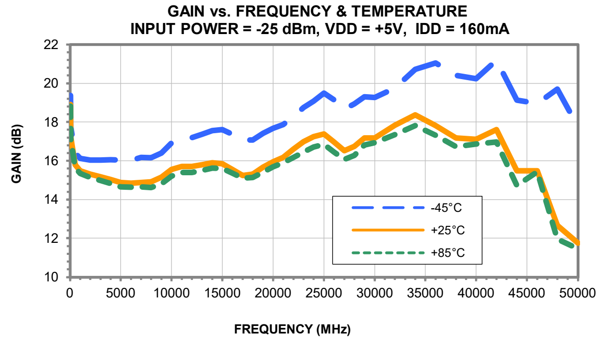
Typical gap of 76μm (3mils) between edge of die and edge of ground pad.

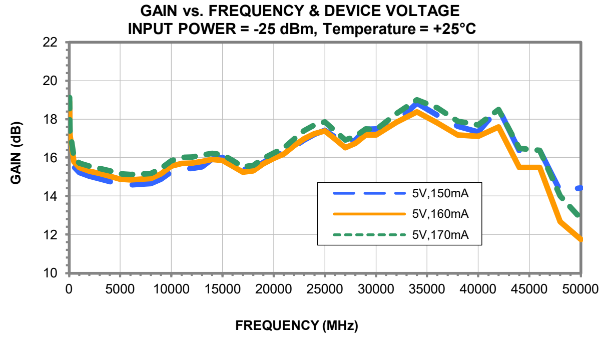
FIG. 3 OUTPUT POWER VS. VDET

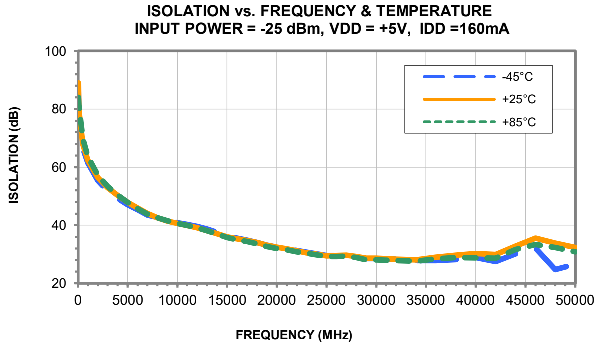


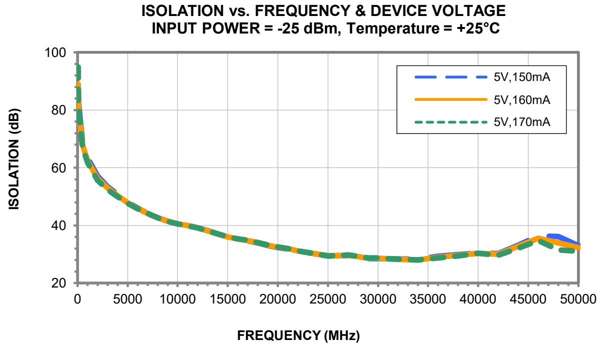
ASSEMBLY PROCEDURE

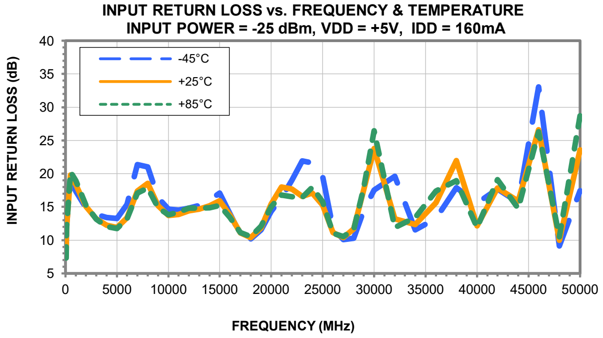
1. Storage
   Die should be stored in a dry nitrogen purged desiccators or equivalent.
2. ESD
   MMIC PHEMT amplifier die are susceptible to electrostatic and mechanical damage. Die are supplied in antistatic protected material, which should be open in clean room conditions at an appropriately grounded anti-static workstation.
3. Die Handling and Attachment
   Devices need careful handling using correctly designed collets, it is recommended to handle the chip along the edges with a custom design collet. The die mounting surface must be clean and flat. Using conductive silver filled epoxy, recommended epoxies are Ablestik 84-1 LMISR4 or equivalents. Apply sufficient epoxy to meet required epoxy bond line thickness, epoxy fillet height and epoxy coverage around total periphery. Parts shall be cured in a nitrogen filled atmosphere per manufacturer's cure condition. The surface of the chip has exposed air bridges and should not be touched with vacuum collet, tweezers or fingers.
4. Wire Bonding
   Bond pad openings in the surface passivation above the bond pads are provided to allow wire bonding to the die gold bond pads. Thermo-sonic bonding is used with minimized ultrasonic content. Bond force, time, ultrasonic power and temperature are all critical parameters. Suggested wire is pure gold, 1mil diameter. Bonds must be made from the bond pads on the die to the packaged or substrate. All bond wire length and bond wire height should be kept as short as possible unless specified by the Assembly Drawing to minimize performance degradation due to undesirable series inductance.

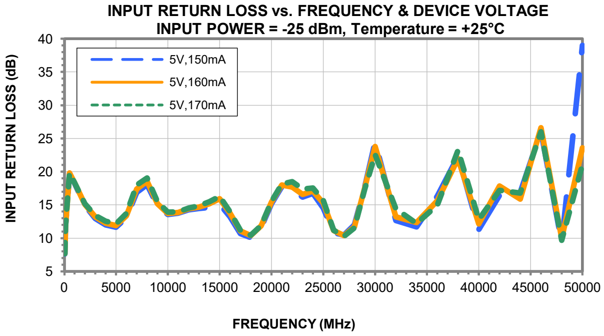

GAIN vs. FREQUENCY & TEMPERATURE
INPUT POWER = -25 dBm, VDD = +5V, IDD = 160mA

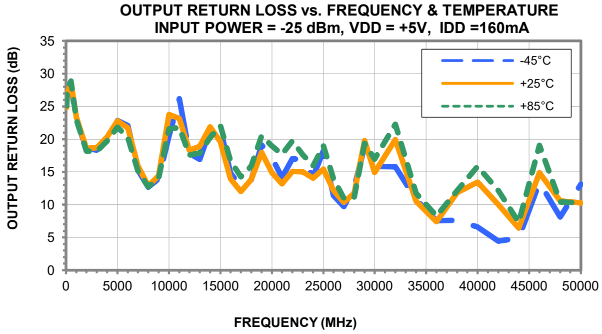

GAIN vs. FREQUENCY & DEVICE VOLTAGE
INPUT POWER = -25 dBm, Temperature = +25°C

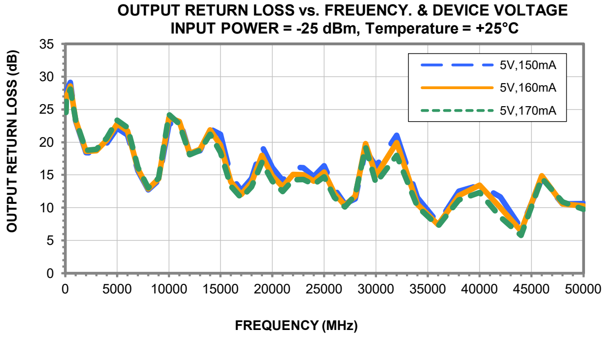

ISOLATION vs. FREQUENCY & TEMPERATURE
INPUT POWER = -25 dBm, VDD = +5V, IDD =160mA


ISOLATION vs. FREQUENCY & DEVICE VOLTAGE
INPUT POWER = -25 dBm, Temperature = +25°C

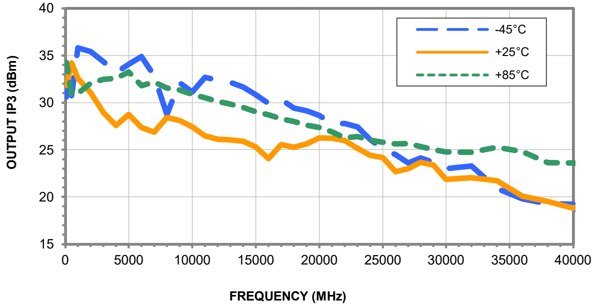

INPUT RETURN LOSS vs. FREQUENCY & TEMPERATURE
INPUT POWER = -25 dBm, VDD = +5V, IDD = 160mA


INPUT RETURN LOSS vs. FREQUENCY & DEVICE VOLTAGE
INPUT POWER = -25 dBm, Temperature = +25°C

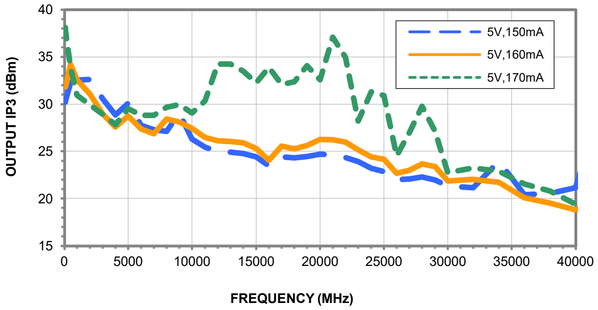

OUTPUT RETURN LOSS vs. FREQUENCY & TEMPERATURE
INPUT POWER = -25 dBm, VDD = +5V, IDD =160mA


OUTPUT RETURN LOSS vs. FREUENCY. & DEVICE VOLTAGE
INPUT POWER = -25 dBm, Temperature = +25°C

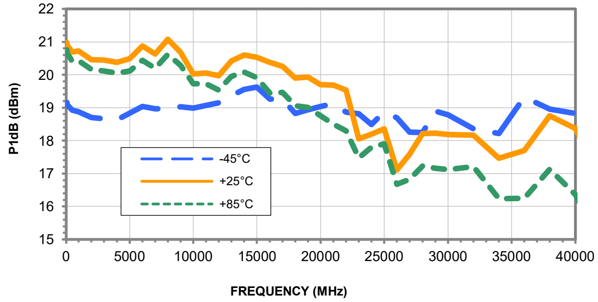
OUTPUT IP3 vs. FREQUENCY & TEMPERATURE
POUT = +5dBm/Tone, VDD = +5V, IDD = 160mA



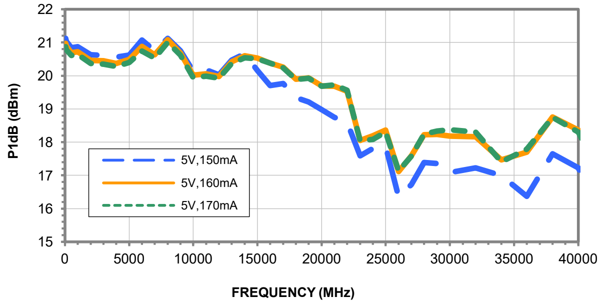
OUTPUT IP3 vs. FREQUENCY & DEVICE VOLTAGE
POUT = +5dBm/Tone, Temperature = +25°C



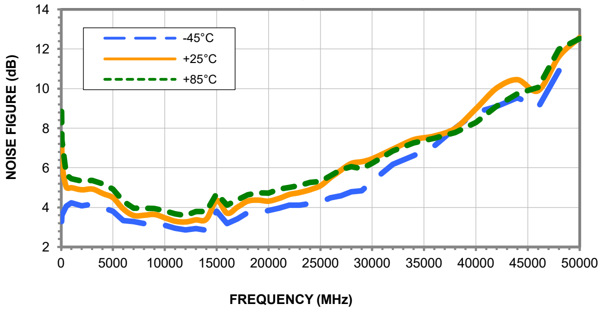
P1dB vs. FREQUENCY & TEMPERATURE
VDD = +5V, IDD = 160mA



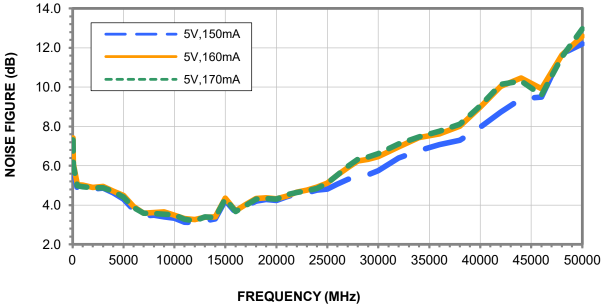
P1dB vs. FREQUENCY & DEVICE VOLTAGE
Temperature = +25°C



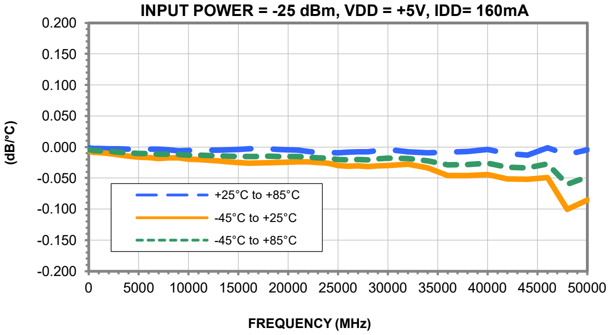
NOISE FIGURE vs. FREQUENCY & TEMPERATURE
VDD = +5V, IDD =160mA



NOISE FIGURE vs. FREQUENCY & DEVICE VOLTAGE
Temperature = +25°C



GAIN VARIATIONs vs. FREQUENCY & TEMPERATURE
INPUT POWER = -25 dBm, VDD = +5V, IDD= 160mA



ADDITIONAL DETAILED TECHNICAL INFORMATION IS AVAILABLE ON OUR DASH BOARD.

Performance Data	Data Table Swept Graphs S-Parameter (S2P Files) Data Set with and without port extension(.zip file)	
Case Style	Die	
Die Ordering and packaging information	Quantity, Package	Model No.
	Gel – Pak: 5, 10, 50, 100, KGD*	AVA-054-DG+
	Medium†, Partial wafer: KGD*<768	AVA-054-DP+
	Full Wafer	AVA-054-DF+
	†Available upon request contact sales representative Refer to AN-60-067	
Die Marking	EL-AMP-13	
Environmental Ratings	ENV80	

*Known Good Die ('KGD') means that the die in question have been subjected to Mini-Circuits DC test performance criteria and measurement instructions and that the parametric data of such die fall within predefined range. While DC testing is not definitive, it does provide a higher degree of confidence that die are capable of meeting typical RF electrical parameters specified by Mini-Circuits.

NOTES

A. Performance and quality attributes and conditions not expressly stated in this specification document are intended to be excluded and do not form a part of this specification document.

B. Electrical specifications and performance data contained in this specification document are based on Mini-Circuit's applicable established test performance criteria and measurement instructions.

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