DOCSIS 3.1

# Power Doubler Hybrid Module ADCA3952

75Ω 45 to 1218 MHz

## FEATURES

- **Total composite power: 73.3 dBmV**
- **High power gain: 25.0 dB at 1218 MHz**
- **Excellent linearity**
- **Very low distortion**
  - **Composite triple beat: –80 dBc typical**
  - **Composite second-order: –78 dBc typical**
  - **Carrier to intermodulation noise: 58 dB typical**
- **Low noise figure: 3 dB at 45 MHz and 4 dB at 1218 MHz**
- **Unconditionally stable**
- **Transient and surge protection**
- **Configurable current: 250 mA to 490 mA at 24 V**

## APPLICATIONS

- **45 MHz to 1218 MHz community access television (CATV) infrastructure amplifier systems**
- **Remote physical layer (PHY)**
- **DOCSIS 3.1 compliant**

## GENERAL DESCRIPTION

The Mini-Circuits' ADCA3952 is a power doubler hybrid module packaged in the industry-standard SOT-115J package. The device achieves high RF output, up to 73.3 dBmV total composite power with 9 dB tilt, by using advanced circuit design techniques, such as gallium arsenide (GaAs), pseudomorphic high electron transistor (pHEMT), and gallium nitride (GaN) HEMT technologies. The dc current can be adjusted externally for optimum distortion performance vs. power consumption over a range of output levels. The ADCA3952 provides high gain, simplifying the design and manufacturing of DOCSIS 3.1™ infrastructure equipment.

This part was acquired by Mini-Circuits from Analog Devices on April 12, 2024.

## FUNCTIONAL BLOCK DIAGRAM

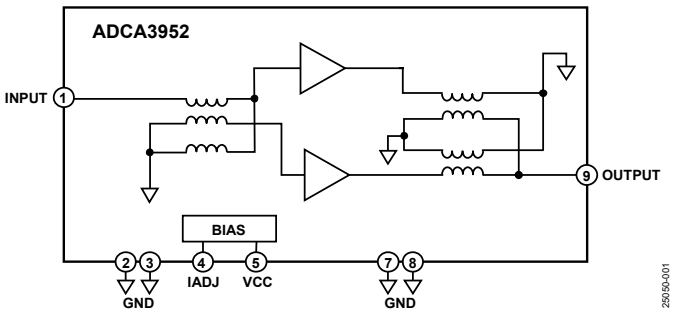


*Figure 1.*

REV. A
ECO-021744
ADCA3952
MCL NY
240508

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## REVISION HISTORY

**4/2024 - Revision A: Transferred from Analog Devices to Mini-Circuits**

**11/2020—Revision 0: Initial Version**

# SPECIFICATIONS

## GENERAL PERFORMANCE

Supply voltage ($V_{CC}$) = 24 V, flange temperature ($T_{FLANGE}$) = 35°C, source impedance ($Z_S$) = load impedance ($Z_L$) = 75 Ω, and IADJ (Pin 4) floating, unless otherwise noted.

**Table 1.**

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| POWER GAIN | S21 | | 23.5 | | dB | Frequency = 45 MHz |
| | | | 25.0 | | dB | Frequency = 1218 MHz |
| SLOPE STRAIGHT LINE [1] | | | 1.0 | | dB | Frequency = 45 MHz to 1218 MHz |
| FLATNESS OF FREQUENCY RESPONSE [2] | | | 0.6 | | dB | Frequency = 45 MHz to 1218 MHz |
| REVERSE ISOLATION | S12 | | −28 | | dB | Frequency = 45 MHz to 1218 MHz |
| RETURN LOSS | | | | | | See Figure 3 and Figure 6 |
| Input | S11 | | −20 | | dB | Frequency = 45 MHz to 320 MHz |
| | | | −18 | | dB | Frequency = 320 MHz to 640 MHz |
| | | | −18 | | dB | Frequency = 640 MHz to 870 MHz |
| | | | −18 | | dB | Frequency = 870 MHz to 1000 MHz |
| | | | −16 | | dB | Frequency = 1000 MHz to 1218 MHz |
| Output | S22 | | −20 | | dB | Frequency = 45 MHz to 320 MHz |
| | | | −20 | | dB | Frequency = 320 MHz to 640 MHz |
| | | | −20 | | dB | Frequency = 640 MHz to 870 MHz |
| | | | −20 | | dB | Frequency = 870 MHz to 1000 MHz |
| | | | −18 | | dB | Frequency = 1000 MHz to 1218 MHz |
| NOISE FIGURE | | | 3 | | dB | Frequency = 45 MHz |
| | | | 4 | | dB | Frequency = 1218 MHz |
| SUPPLY | | | | | | See the Applications Information section for adjusting the bias current and impact on performance |
| Maximum Operating Voltage | $V_{CC}$ | | 24 | 26 | V | |
| DC Current (Total) | $I_{CC\ (TOTAL)}$ | 250 | 470 | 490 | mA | |

[1] Slope straight line is defined as the delta between the gain at the start frequency and the gain at the stop frequency.
[2] Flatness of frequency response is defined as the delta between the gain at any frequency between the start and stop frequencies and a straight line reference drawn between the gain at the start frequency and the gain at the stop frequency.

## DISTORTION DATA (40 MHz TO 550 MHz), ERROR RATES, AND TOTAL COMPOSITE POWER

$V_{CC}$ = 24 V, $T_{FLANGE}$ = 35°C, $Z_S$ = $Z_L$ = 75 Ω, and IADJ (Pin 4) floating, unless otherwise noted.

**Table 2.**

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| DISTORTION | | | | | | Total composite power = 72.4 dBmV, 9 dB extrapolated tilt, 79 continuous wave channels plus 111 digital channels, National Television System Committee (NTSC) frequency raster = 55.25 MHz to 547.25 MHz, −6 dB offset |
| Composite Triple Beat | CTB | | −80 | | dBc | Defined by the National Cable and Telecommunications Association (NCTA) |
| Composite Second-Order | CSO | | −78 | | dBc | Defined by NCTA |
| Carrier to Intermodulation Noise | | | 58 | | dB | Defined by American National Standard/Society of Cable Telecommunications Engineers (ANSI/SCTE) 17 (test procedure for carrier to noise) |
| ERROR RATES | | | | | | Total composite power = 72.4 dBmV, 9 dB extrapolated tilt, 190 digital (256 QAMs) channels |
| Bit Error Ratio | BER | | $<1 \times 10^{-9}$ | | | PreViterbi |
| TOTAL COMPOSITE POWER | TCP | | 73.3 | | dBmV | 9 dB tilt, see Figure 9 and Figure 10 |

## ABSOLUTE MAXIMUM RATINGS

**Table 3.**

| Parameter | Rating |
|---|---|
| $V_{CC}$ | |
| DC Supply over Voltage (5 Minute) | 28 V |
| RF Input Voltage ($RF_{INPUT}$), Single Tone | 75 dBmV |
| IADJ Voltage ($V_{IADJ}$) | −1 V to +26 V |
| Operating Temperature Range | |
| $T_A$ | −30°C to +85°C |
| $T_{FLANGE}$ | −30°C to +100°C |
| Storage Temperature ($T_S$) Range | −40°C to +100°C |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

**ESD CAUTION**

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

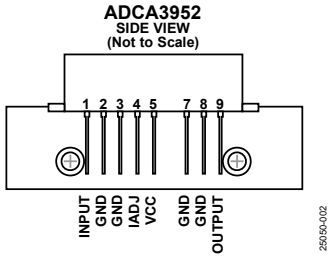


*Figure 2. Pin Configuration*

**Table 4. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | INPUT | RF Input |
| 2, 3 | GND | Ground |
| 4 | IADJ | Bias Control Pin |
| 5 | VCC | Positive Supply Voltage, 24 V Typical |
| 7, 8 | GND | Ground |
| 9 | OUTPUT | RF Output |

## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{CC}$ = 24 V, $T_{FLANGE}$ = 35°C, $Z_S$ = $Z_L$ = 75 Ω, and IADJ (Pin 4) floating, unless otherwise noted.

### S-PARAMETERS

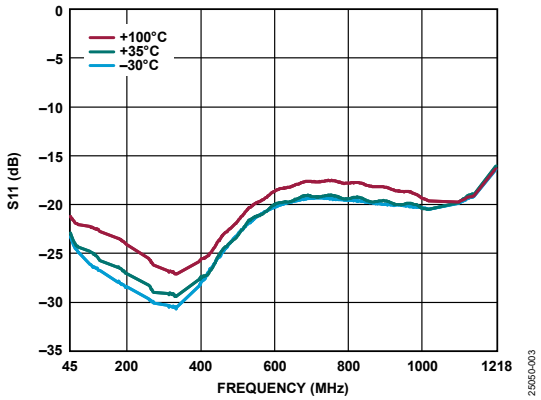


*Figure 3. S11 vs. Frequency at Various Temperatures*

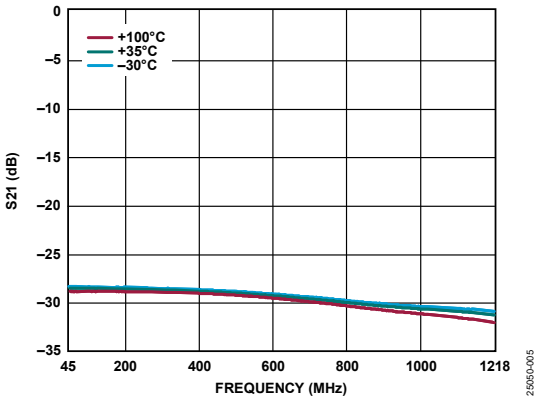


*Figure 5. S12 vs. Frequency at Various Temperatures*

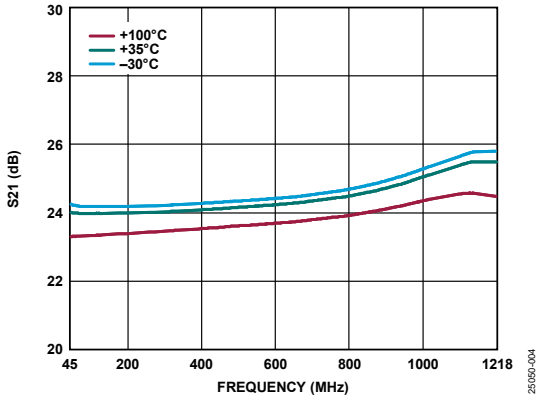


*Figure 4. S21 vs. Frequency at Various Temperatures*

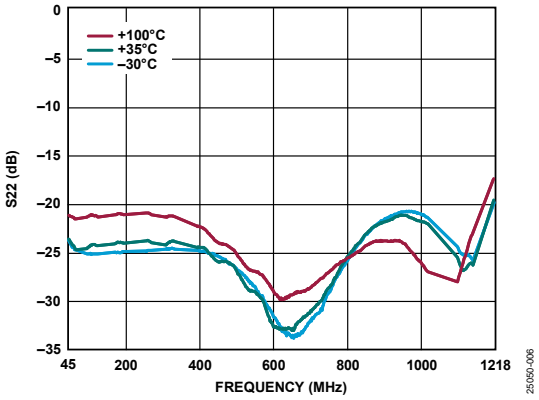


*Figure 6. S22 vs. Frequency at Various Temperatures*

## 9 dB TILT PERFORMANCE

9 dB extrapolated tilt, and 190 digital channels (QAM256, ITU-T J.83, Annex B).

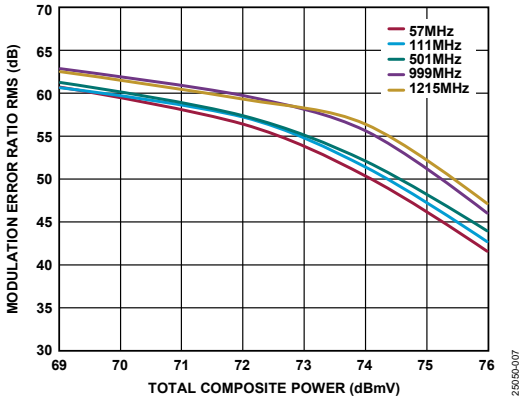


*Figure 7. Modulation Error Ratio RMS vs. Total Composite Power at Various Frequencies, 35°C, 9 dB Tilt*

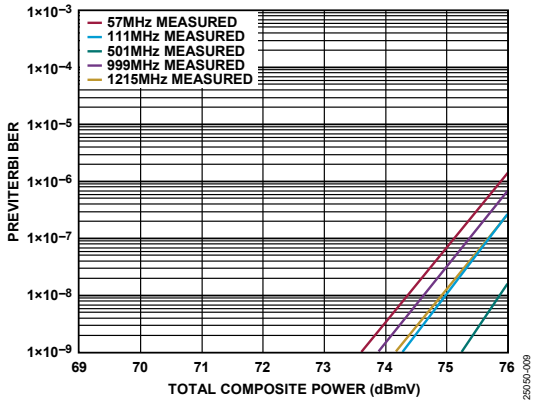


*Figure 9. PreViterbi BER vs. Total Composite Power at Various Frequencies, 35°C, 9 dB Tilt*

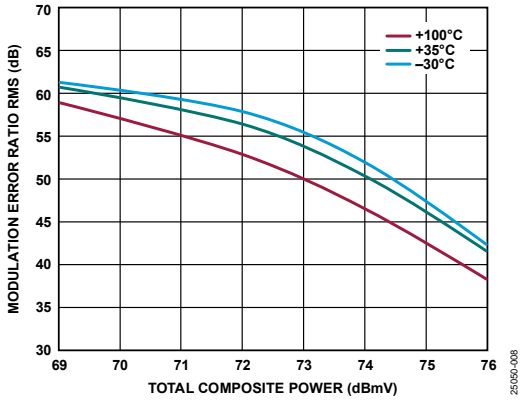


*Figure 8. Modulation Error Ratio RMS vs. Total Composite Power at Various Temperatures, 57 MHz, 9 dB Tilt*

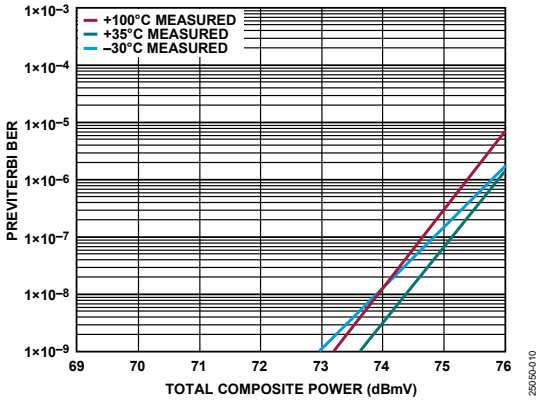


*Figure 10. PreViterbi BER vs. Total Composite Power at Various Temperatures, 57 MHz, 9 dB Tilt*

## THEORY OF OPERATION

The ADCA3952 is a 75 Ω input and output matched module designed for CATV applications. The ADCA3952 uses cascode field effect transistor (FET) feedback amplifiers in a Class A, push pull configuration. The bottom half of the cascode stages are implemented in a single die, linear FET process that minimizes parasitics, thereby enabling higher gain. The top devices in the cascodes are implemented using a linear GaN process able to swing high RF voltages. The frequency of operation is from 45 MHz to 1218 MHz.

Internally, the ADCA3952 module uses a balun to convert the input signal to a balanced signal that feeds the active stages. An output impedance transformer and balun combination converts the balanced GaN signals to an unbalanced 75 Ω output. The output transformer also feeds the dc to the active stages and cancels second-order distortion products coming from the active devices.

The module has a bias control pin (IADJ) that can set the dc current consumption from low bias to the full bias of the device by connecting a resistor from the IADJ pin to ground or by the use of a positive voltage.

The ADCA3952 is unconditionally stable and includes transient and surge protection circuits for robust operation in systems targeting DOCSIS 3.1 and legacy DOCSIS standards.

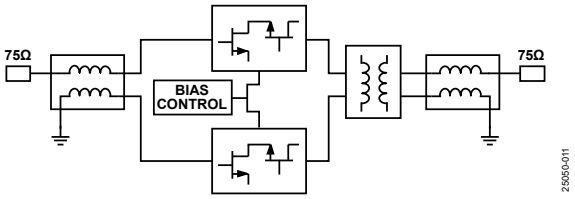


*Figure 11. Simplified Schematic*

## APPLICATIONS INFORMATION

Basic connections for operating the ADCA3952 are shown in Figure 14. Both the INPUT pin (Pin 1) and the OUTPUT pin (Pin 9) of the ADCA3952 are matched to 75 Ω. The VCC pin (Pin 5) requires 24 V for typical operation. It is recommended to leave the IADJ pin (Pin 4) open for full bias operation. For bias control on the ADCA3952 supply current, apply an external control voltage between −0.6 V and +1 V at the IADJ pin. Figure 12 illustrates the typical supply current over the control voltages at the IADJ pin of the ADCA3992.

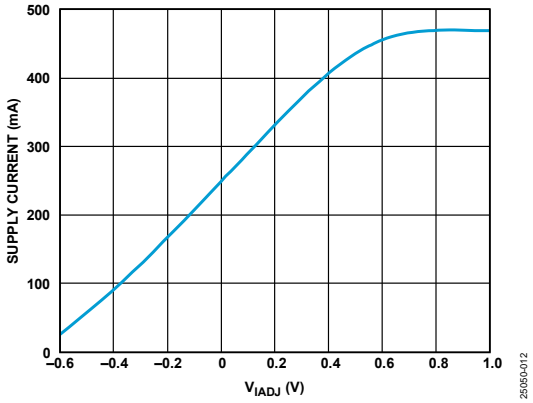


*Figure 12. Supply Current vs. $V_{IADJ}$ at the IADJ Pin*

In systems that require the bias current to be lower than the default but it is not critical, a resistor can be placed between the IADJ pin (Pin 4 ) and ground to set the current (see Figure 15). Figure 13 illustrates the typical supply current of the ADCA3952 in this configuration for a range of resistor values between 100 Ω and 40 kΩ.

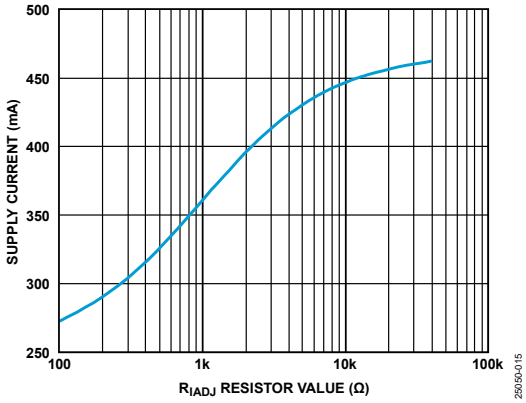


*Figure 13. Supply Current vs. $R_{IADJ}$ Resistor Value*

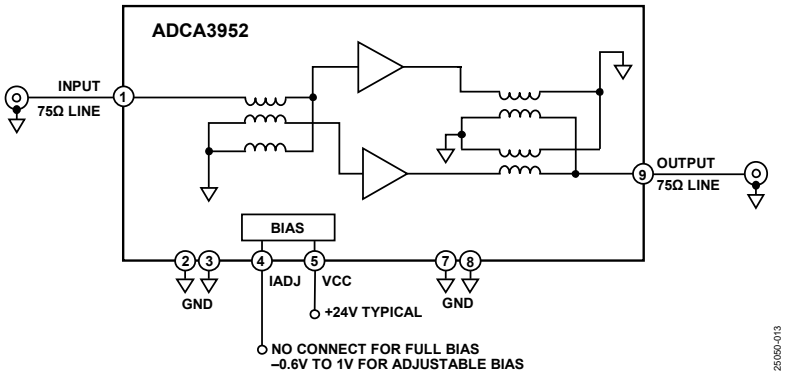


*Figure 14. Basic Connections*

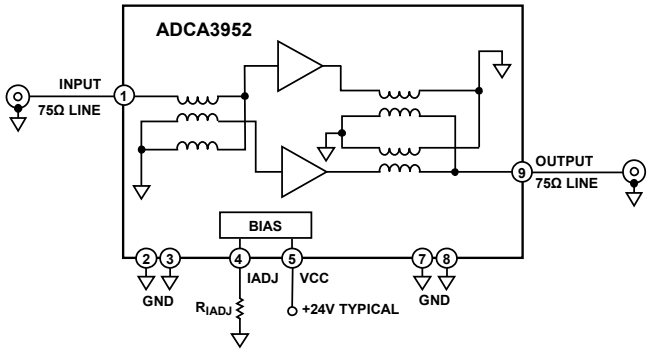


*Figure 15. IADJ Bias Control Connections*

The ADCA3952 employs a versatile circuit design, allowing system designers to configure the supply voltage at the VCC connection (Pin 5) and the bias control voltage at the IADJ connection (Pin 4) to optimize the power dissipation in any given application. Figure 16 illustrates the modulation error ratio performance trade-off for different bias current configurations.

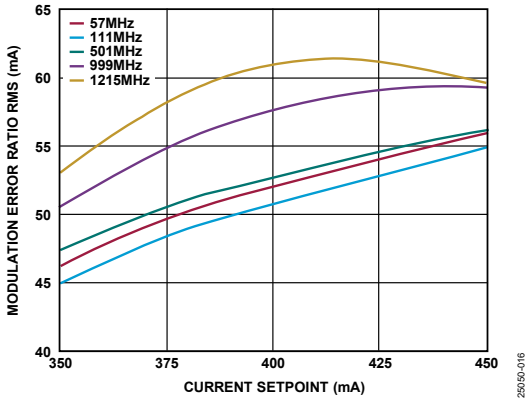


*Figure 16. Modulation Error Ratio RMS vs. Current Setpoint for Various Frequencies, Bias = 24 V, 35°C, 9 dB Tilt, Total Composite Power = 72.0 dBmV*

## OUTLINE DIMENSIONS

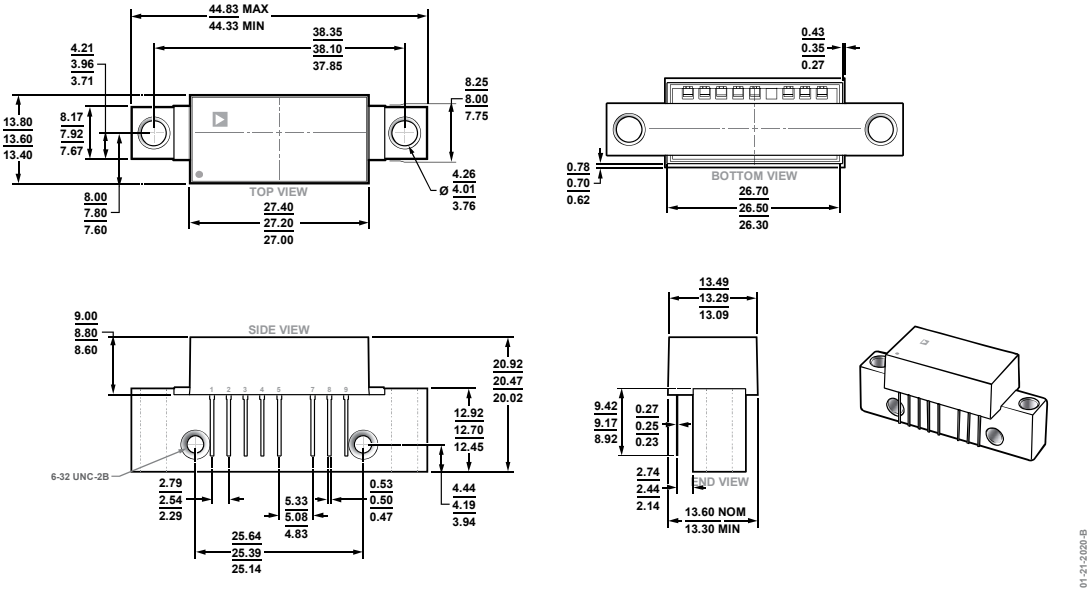


*Figure 17. 8-Pin SOT-115J Module Package [MODULE]*
*(ML-8-1)*
*Dimensions shown in millimeters*

### ORDERING GUIDE

| Model [1] | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| ADCA3952AMLZ | −30°C to +100°C | 8-Pin SOT-115J Module Package [MODULE], Box with 25 Pieces | ML-8-1 |

[1] Z = RoHS Compliant Part.

NOTES

A. Performance and quality attributes and conditions not expressly stated in this specification document are intended to be excluded and do not form a part of this specification document.
B. Electrical specifications and performance data contained in this specification document are based on Mini-Circuit's applicable established test performance criteria and measurement instructions.
C. The parts covered by this specification document are subject to Mini-Circuits standard limited warranty and terms and conditions (collectively, "Standard Terms"); Purchasers of this part are entitled to the rights and benefits contained therein. For a full statement of the standard terms and the exclusive rights and remedies thereunder, please visit Mini-Circuits' website at www.minicircuits.com/terms/viewterm.html