

Surface Mount Digital Step Attenuator

DAT-3175A Series

75Ω 0 to 31 dB, 1.0 dB Step 1MHz to 2.5 GHz



CASE STYLE: DG983-2

The Big Deal

- Wideband, operates up to 2.5 GHz
- Glitchless attenuation transitions
- High IP3, 52 dBm

Product Overview

The DAT-3175A+ series of 75Ω digital step attenuators provides adjustable attenuation from 0 to 31 dB in 1.0 dB steps. The control is a 5-bit serial/parallel interface, and the attenuators operate with either single positive or dual (positive and negative) supply voltage. DAT-3175A+ series models are produced by a unique CMOS process on silicon, offering the performance of GaAs with the advantages of conventional CMOS devices.

Key Features

Feature	Advantages
Wideband operation, specified from 1MHz to 2.5 GHz	Can be used in multiple applications such as various versions of DOCSIS, satellite and defense, reducing part count.
Serial or parallel interface	Models available with serial or parallel interface mode to suit customer demand.
Good VSWR, 1.3:1 typ.	Eases interfacing with adjacent components and results in low amplitude ripple.
Single positive supply models: (Model suffixes: -SP+ and -PP+) +2.3 to +3.6V+	Use of single positive supply simplifies power supply design. An internal negative voltage generator supplies the desired negative voltage. Single positive supply results in excellent spurious performance, -140 dBm typical.
Dual supply models: (Model suffixes: -SN+ and -PN+) +2.7 to +3.6V (Positive) and -3.6 to -3.2V (Negative)	Dual supply provides spurious-free operation. It also allows fast switching up to 1 MHz (vs. 25 kHz for single supply).
Useable over a wide range of supply voltages, +2.3/2.7 to 5.2V	Wide range of positive operating voltages allows the DAT-3175A+ Series of models to be used in a wide range of applications. See Application Note AN-70-032 for operation above +3.6V
Footprint compatible to DAT-3175-XX+ Series (XX=SN/SP/PN/PP)	Can fit into existing footprint and provide wideband performance, to 2.5 GHz instead of 2.0 GHz.
Glitchless Attenuation Transitions, 0.26 typical	Compared to previous generation of digital attenuators which is a vast improvement.

Digital Step Attenuator

75Ω 1-2500 MHz

31 dB, 1.0 dB Step

5 Bit, Serial Control Interface, Single Supply Voltage

Product Features

- Single positive supply voltage
- Immune to latch up
- Glitchless attenuation transitions
- Excellent accuracy, 0.1 dB Typ
- Low Insertion Loss
- High IP3, +55-59 dBm Typ
- Very low DC power consumption
- Excellent return loss, 18 dB Typ
- Small size 4.0 x 4.0 mm

Typical Applications

- DOCSIS® 3.1
- Portable Wireless
- CATV & DBS
- MMDS & Wireless LAN
- Wireless Local Loop
- UNII & Hiper LAN
- Power amplifier distortion canceling loops



Generic photo used for illustration purposes only

DAT-3175A-SP+

CASE STYLE: DG983-2

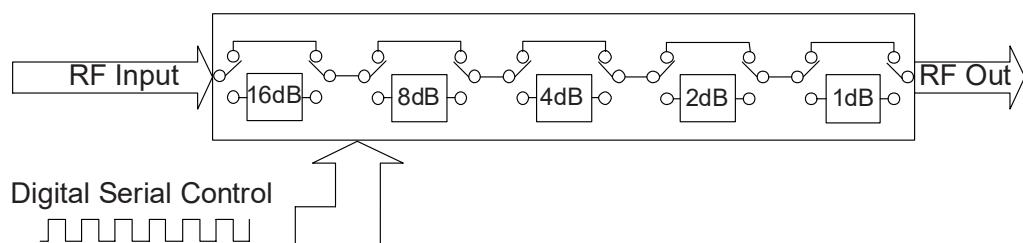
+RoHS Compliant

The +Suffix identifies RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications

General Description

The DAT-3175A-SP+ is a 75Ω RF digital step attenuator that offers an attenuation range up to 31 dB in 1.0 dB steps. The control is a 5-bit serial interface, operating on single (positive) supply voltage. The DAT-3175A-SP+ is produced using a unique CMOS process on silicon, offering the performance of GaAs, with the advantages of conventional CMOS devices.

Simplified Schematic



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Digital Step Attenuator

DAT-3175A-SP+

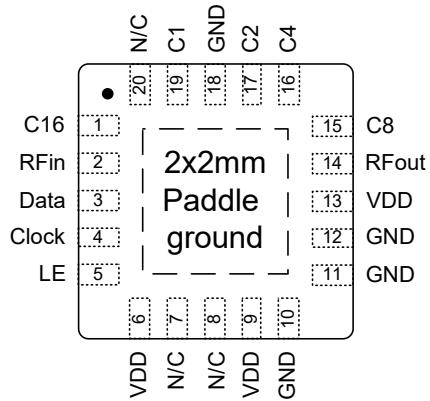
Pin Description

Function	Pin Number	Description
C16	1	Control for Attenuation bit, 16dB (Notes 4,7)
RF in	2	RF in port (Note 1)
Data	3	Serial Interface data input (Note 3)
Clock	4	Serial Interface clock input
LE	5	Latch Enable Input (Note 2)
V _{DD}	6	Power Supply
N/C	7	Not connected
N/C	8	Not connected
V _{DD}	9	Power Supply
GND	10	Ground connection
GND	11	Ground connection
GND	12	Ground connection (Note 7)
V _{DD}	13	Power Supply
RF out	14	RF out port (Note 1)
C8	15	Control for attenuation bit, 8 dB (Note 4)
C4	16	Control for attenuation bit, 4 dB (Note 4)
C2	17	Control for attenuation bit, 2 dB (Note 4)
GND	18	Ground Connection
C1	19	Control for attenuation bit, 1 dB (Note 4)
N/C	20	Not connected (Note 7,8)
GND	Paddle	Paddle ground (Note 6)

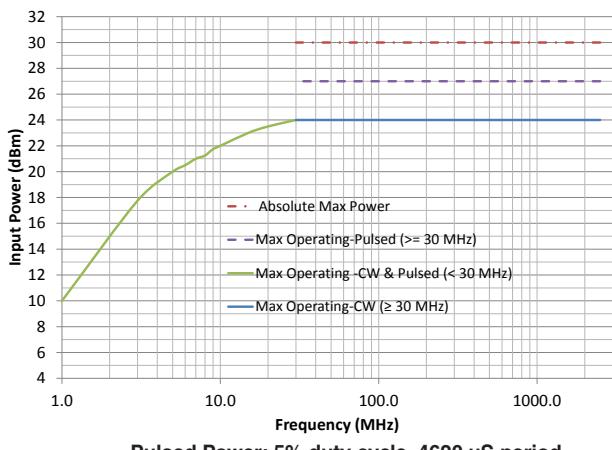
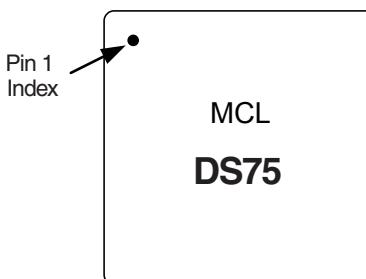
Notes:

1. Both RF ports must be held at 0VDC or DC blocked with an external series capacitor.
2. Latch Enable (LE) has an internal $2M\Omega$ resistor to V_{DD} .
3. Place a $10K\Omega$ resistor in series, as close to pin as possible to avoid freq. resonance.
4. Refer to Power-up Control Settings.
5. The exposed solder pad on the bottom of the package (See Pin configuration) must be grounded for proper device operation.
6. Ground must be less than 80 mil (0.08") from Pin 12 for proper device operation.
7. This pin has internal $1M\Omega$ pull down resistor to ground.
8. Place $10K\Omega$ resistor to ground externally.

Pin Configuration (Top View)



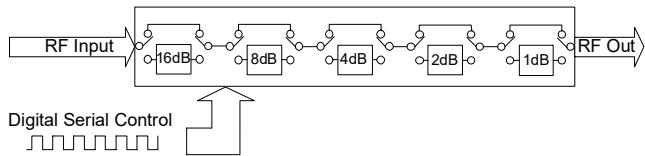
Device Marking



Digital Step Attenuator

DAT-3175A-SP+

Simplified Schematic



The DAT-3175A-SP+ serial interface consists of 5 control bits that select the desired attenuation state, as shown in Table 1: Truth Table

Table 1. Truth Table

Attenuation State	C16	C8	C4	C2	C1
Reference	0	0	0	0	0
1 (dB)	0	0	0	0	1
2 (dB)	0	0	0	1	0
4 (dB)	0	0	1	0	0
8 (dB)	0	1	0	0	0
16 (dB)	1	0	0	0	0
31 (dB)	1	1	1	1	1

Note: Not all 32 possible combinations of C1 - C16 are shown in table

The serial interface is a 5-bit serial in, parallel-out shift register buffered by a transparent latch.

It is controlled by three CMOS-compatible signals: Data, Clock, and Latch Enable (LE). The Data and Clock inputs allow data to be serially entered into the shift register, a process that is independent of the state of the LE input.

The LE input controls the latch. When LE is HIGH, the latch is transparent and the contents of the serial shift register control the attenuator. When LE is brought LOW, data in the shift register is latched.

The shift register should be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input should then be toggled HIGH and brought LOW again, latching the new data. The timing for this operation is defined by **Figure 3** (Serial Interface Timing Diagram) and **Table 2** (Serial Interface AC Characteristics).

Figure 3: Serial Interface Timing Diagram

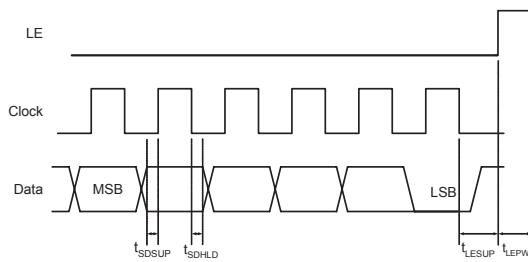


Table 2. Serial Interface AC Characteristics

Symbol	Parameter	Min.	Max.	Units
f_{clk}	Serial data clock frequency (Note 1)		10	MHz
t_{clkH}	Serial clock HIGH time	30		ns
t_{clkL}	Serial clock LOW time	30		ns
t_{LESUP}	LE set-up time after last clock falling edge	10		ns
t_{LEPW}	LE minimum pulse width	30		ns
t_{SDSUP}	Serial data set-up time before clock rising edge	10		ns
t_{SDHLD}	Serial data hold time after clock falling edge	10		ns

Note 1. f_{clk} verified during the functional pattern test. Serial programming sections of the functional pattern are clocked at 10MHz to verify f_{clk} specification.

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The DAT-3175A-SP+, uses a common 5-bit serial word format, as shown in Table 3: 5-Bit attenuator Serial Programming Register Map.

The first bit, the MSB, corresponds to the 16-dB Step and B1 bit corresponds to the 1dB step.

Table 3. 5-Bit attenuator Serial Programming Register Map					
B5	B4	B3	B2	B1	B0
C16	C8	C4	C2	C1	0

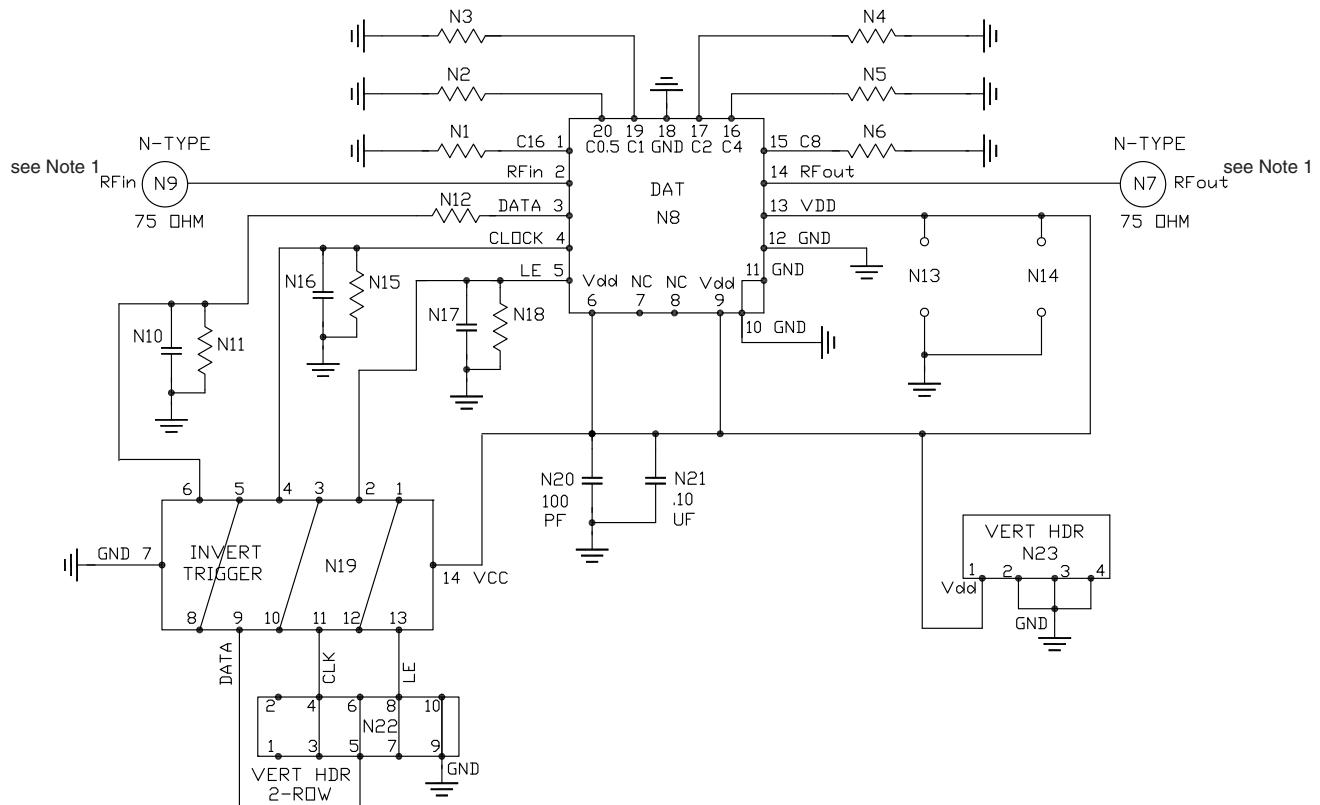
MSB (first in) Note: The stop bit (B0) must always be low to prevent the attenuator from entering an unknown state. LSB (last in)

Power-up Control Settings

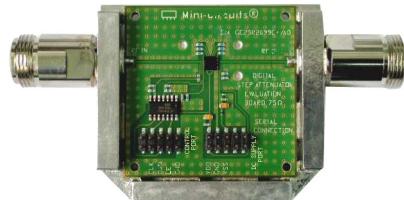
The DAT-3175A-SP+ always assumes a specifiable attenuation setting on power-up, allowing a known attenuation state to be established before an initial serial control word is provided.

When the attenuator powers up, the five control bits are set to whatever data is present on the five data inputs (C1 to C16).

This allows any one of the 32 attenuation settings to be specified as the power-up state.



Note 1: Both RF ports must be held at 0VDC or DC blocked with an external series capacitor.



Bill of Materials	
N1-N6, N11, N12, N15, N18	Resistor 0603 10 KOhm +/- 1%
N10, N16, N17, N20	NPO Capacitor 0603 100pF +/- 5%
N21	Tantalum Capacitor 0805 100nF +/- 10%
N19	Hex Invert Schmitt Trigger MSL1

** N12 can be reduced to 0Ω

TB-344

Additional Detailed Technical Information

additional information is available on our dash board. To access this information [click here](#)

Performance Data	Data Table
	Swept Graphs
	S-Parameter (S2P Files) Data Set (.zip file)
Case Style	DG983-2 Plastic package, exposed paddle, lead finish: NiPdAu
Tape & Reel Standard quantities available on reel	F87 7" reels with 20, 50, 100, 200, 500 Or 1000 devices 13" reels with 3K devices
Suggested Layout for PCB Design	PL-203
Evaluation Board	TB-344
Environmental Ratings	ENV33T1

ESD Rating

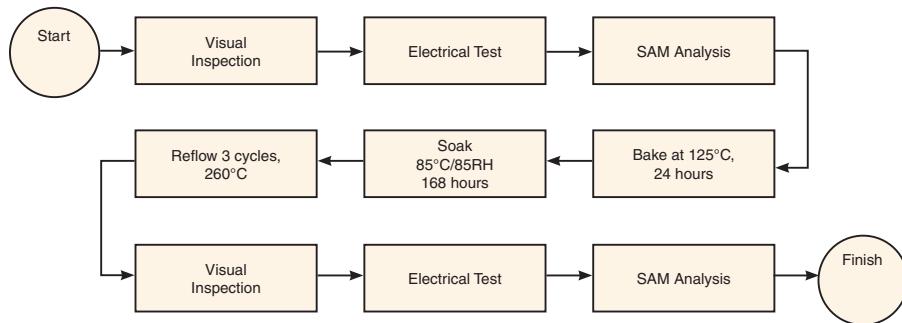
Human Body Model (HBM): Class 1C (1000 to <2000V) in accordance with MIL-STD-883 method 3015 (pass 1500V)

Charge Device Model class C2 (500 to <1000V) per JESD22-C101

MSL Rating

Moisture Sensitivity: MSL1 in accordance with IPC/JEDEC J-STD-020D

MSL Test Flow Chart



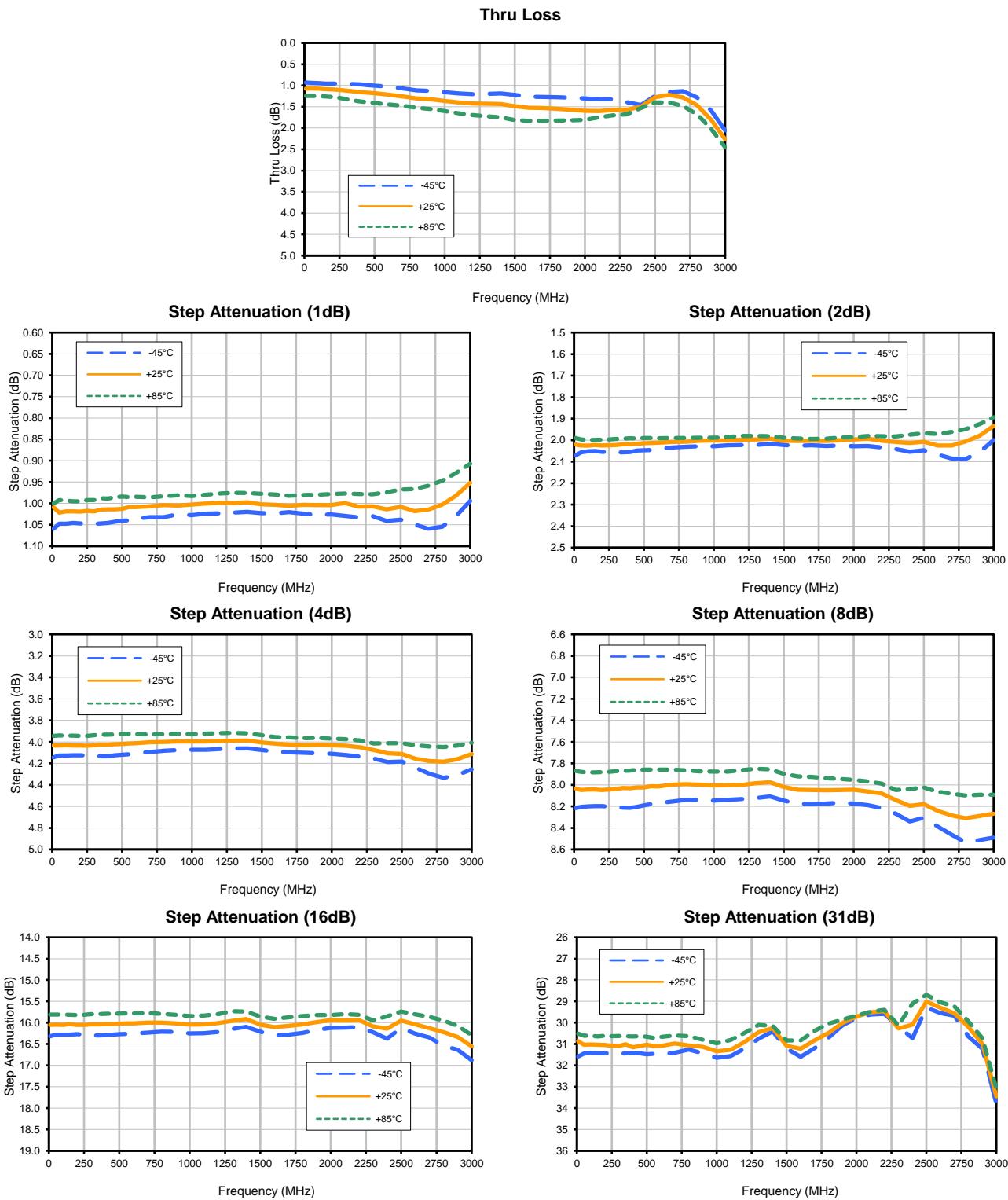
Additional Notes

- Performance and quality attributes and conditions not expressly stated in this specification document are intended to be excluded and do not form a part of this specification document.
- Electrical specifications and performance data contained in this specification document are based on Mini-Circuit's applicable established test performance criteria and measurement instructions.
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Digital Step Attenuator

Typical Performance Curves

DAT-3175A-SP+



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IF/RF MICROWAVE COMPONENTS

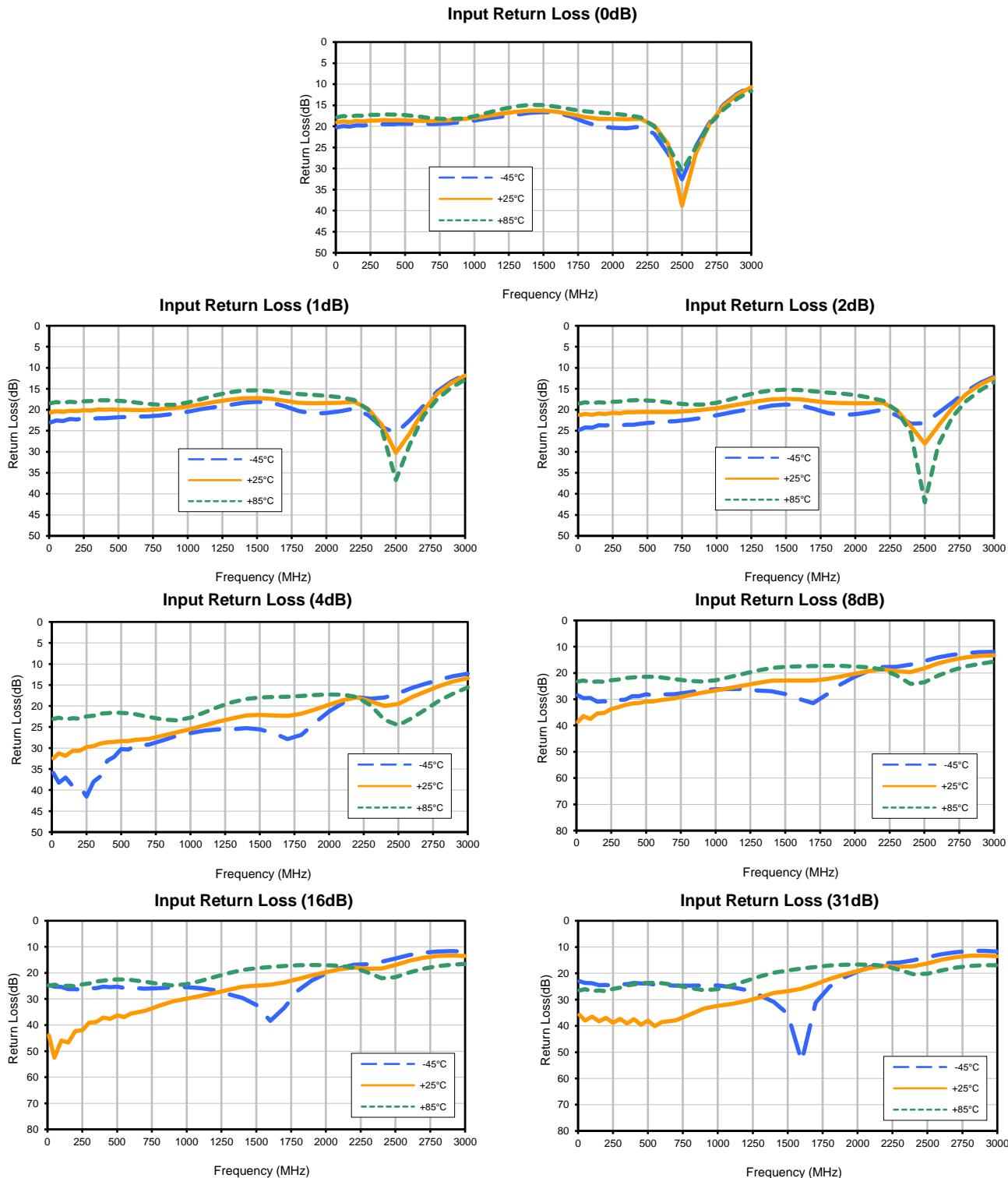
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REV. OR
DAT-3175A-SN+
10/14/2016
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Typical Performance Curves



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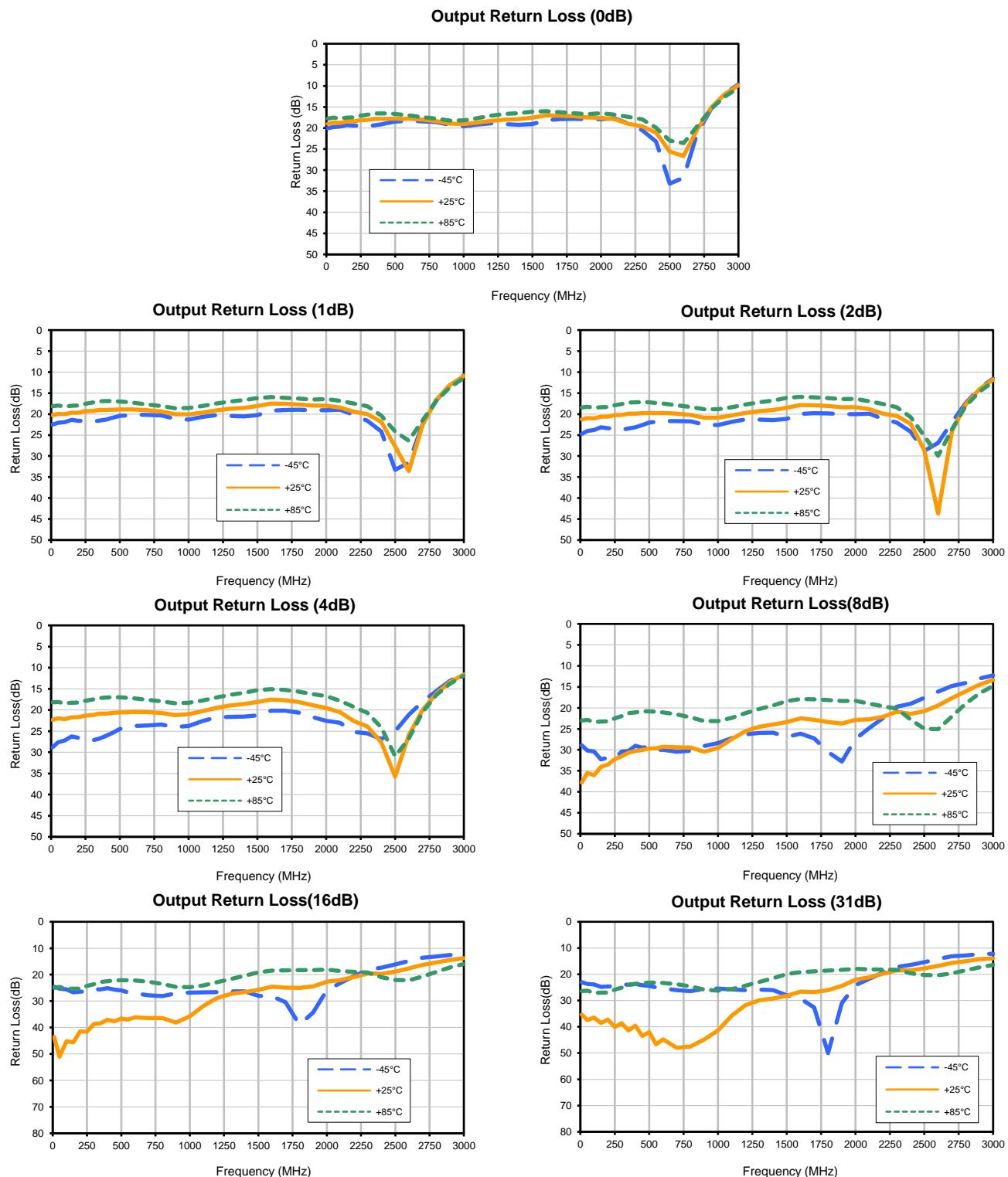
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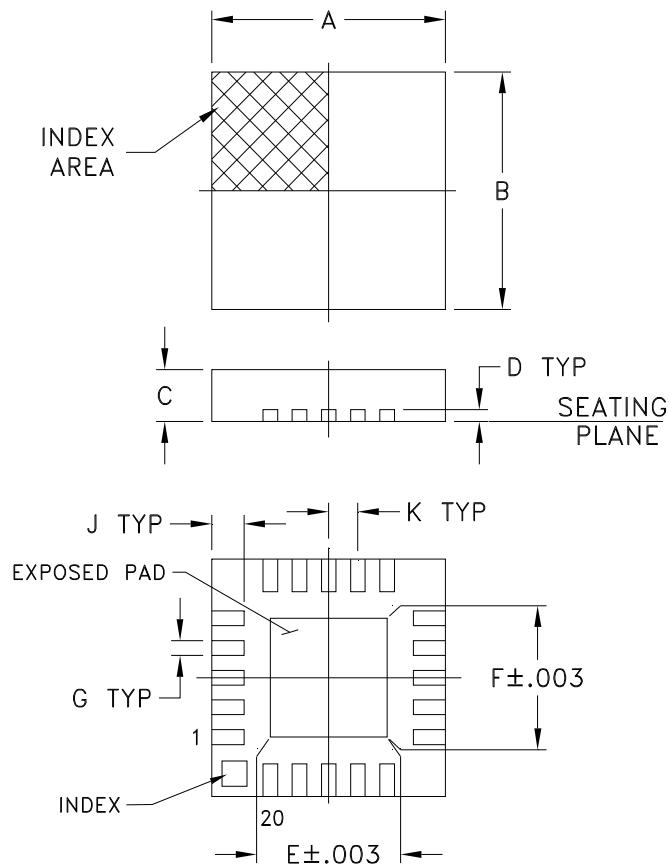
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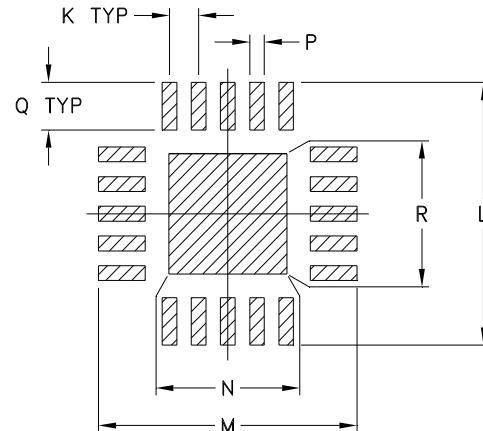
Typical Performance Curves



Outline Dimensions



PCB Land Pattern



CASE #	A	B	C	D	E	F	G	H	J	K
DG983-2	.157 (4.00)	.157 (4.00)	.033 (0.85)	.008 (0.20)	.085 (2.15)	.085 (2.15)	.009 (0.23)	--	.022 (0.55)	.020 (0.50)

CASE #	L	M	N	P	Q	R	WT. GRAM
DG983-2	.177 (4.50)	.177 (4.50)	.081 (2.06)	.010 (0.25)	.032 (0.81)	.081 (2.06)	.04

Dimensions are in inches (mm). Tolerances: 2 Pl. $\pm .01$; 3 Pl. $\pm .005$

Notes:

1. Case material: Plastic.
2. Termination finish:

For RoHS Case Styles: 0.2 μ inches of Gold (Au) over 0.1 μ inch of Palladium (Pd) over 10 μ inches of Nickel (Ni). All models, (+) suffix.

For RoHS-5 Case Styles: Tin-Lead plate. All models, no (+) suffix.

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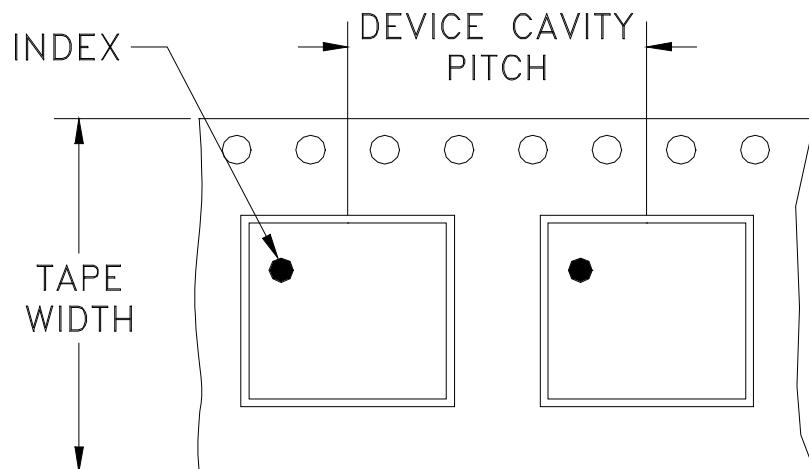


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Tape & Reel Packaging TR-F87

DEVICE ORIENTATION IN T&R



DIRECTION OF FEED

Tape Width, mm	Device Cavity Pitch, mm	Reel Size, inches	Devices per Reel	
12	8	7	Small quantity standards (see note)	20
				50
				100
				200
				500
				1000
		13	Standard	3000

Note : Please Consult individual model data sheet to determine device per reel availability

Mini-Circuits carrier tape materials provide protection from ESD (Electro-Static Discharge) during handling and transportation. Tapes are static dissipative and comply with industry standards EIA-481/EIA-541.

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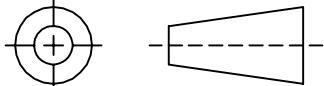
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THIRD ANGLE PROJECTION



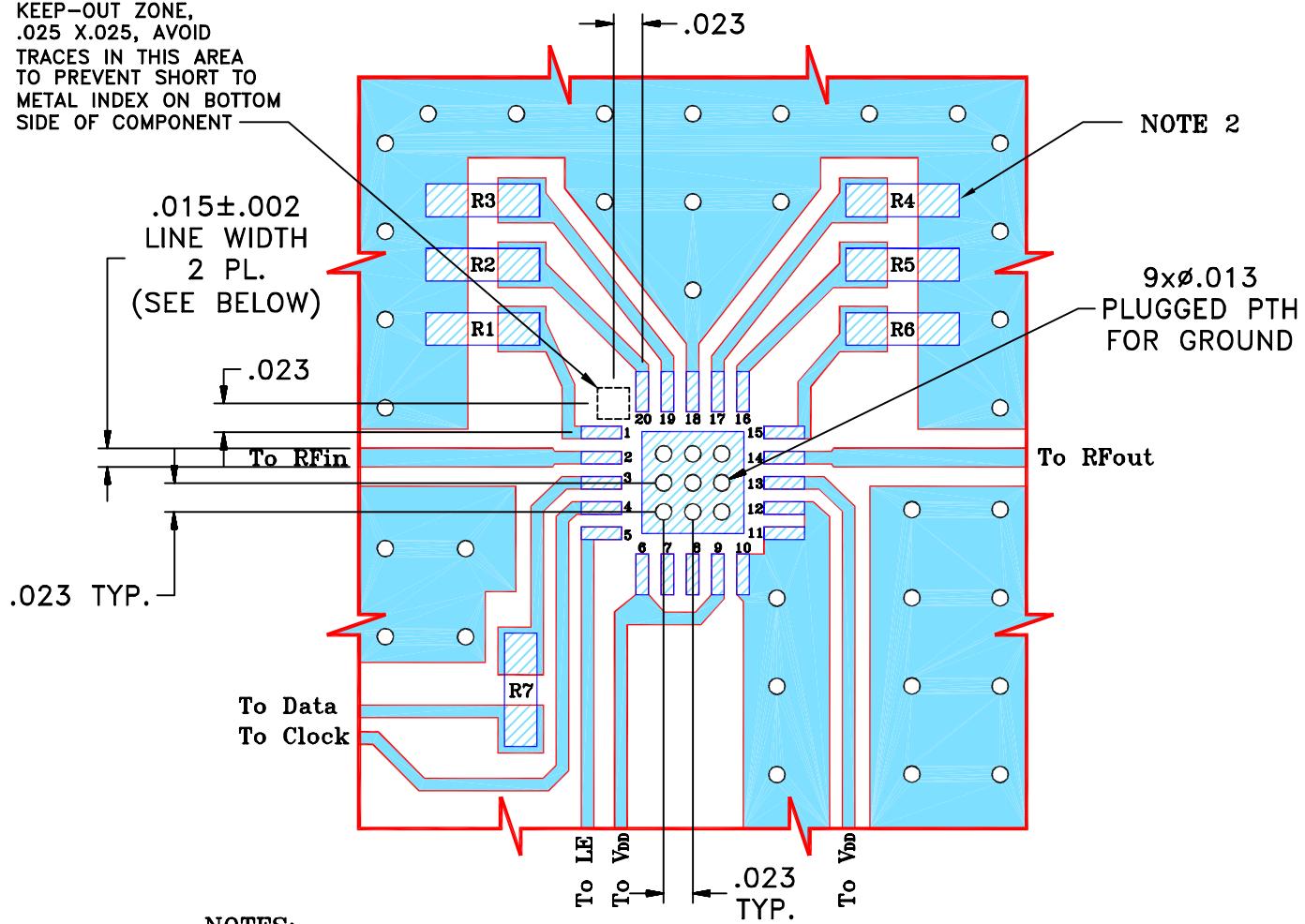
REVISIONS

REV	ECN No.	DESCRIPTION	DATE	DR	AUTH
OR	M97254	NEW RELEASE (FROM RAVON)	03/05	DK	HH
A	M102713	MODIFIED HATCH, NOTES & ADDED "...WITH SMOBC"	01/06	GT	HH
B	M103510	ADD R7 & CHANGE LOCATION DESIGNATORS	07/09	EM	KN
B	R63339	ADD R7 & CHANGE LOCATION DESIGNATORS	07/09	EM	KN

SUGGESTED MOUNTING CONFIGURATION

FOR DG983-1 CASE STYLE, qm PIN CONNECTION, 75Ω .

KEEP-OUT ZONE,
.025 X.025, AVOID
TRACES IN THIS AREA
TO PREVENT SHORT TO
METAL INDEX ON BOTTOM
SIDE OF COMPONENT



NOTES:

1. TRACE WIDTH IS SHOWN FOR FR4 WITH DIELECTRIC THICKNESS $.025'' \pm .002''$. COPPER: 1/2 OZ. EACH SIDE.
FOR OTHER MATERIALS TRACE WIDTH MAY NEED TO BE MODIFIED.
2. 0603 SIZE CHIP FOOT PRINTS SHOWN FOR REFERENCE,
VALUES OF RESISTORS WILL VARY BASED ON APPLICATION.
3. BOTTOM SIDE OF THE PCB IS CONTINUOUS GROUND PLANE.

DENOTES PCB COPPER LAYOUT WITH SMOBC
(SOLDER MASK OVER BARE COPPER)

DENOTES COPPER LAND PATTERN FREE OF SOLDER MASK

UNLESS OTHERWISE SPECIFIED

DIMENSIONS ARE IN INCHES

TOLERANCES ON:

2 PL DECIMALS \pm 3 PL DECIMALS $\pm .005$ ANGLES \pm FRACTIONS \pm

INITIALS

DATE

DRAWN

DK (RAVON)

08 MAR 05

CHECKED

RZ (RAVON)

08 MAR 05

APPROVED

HH (RAVON)

08 MAR 05

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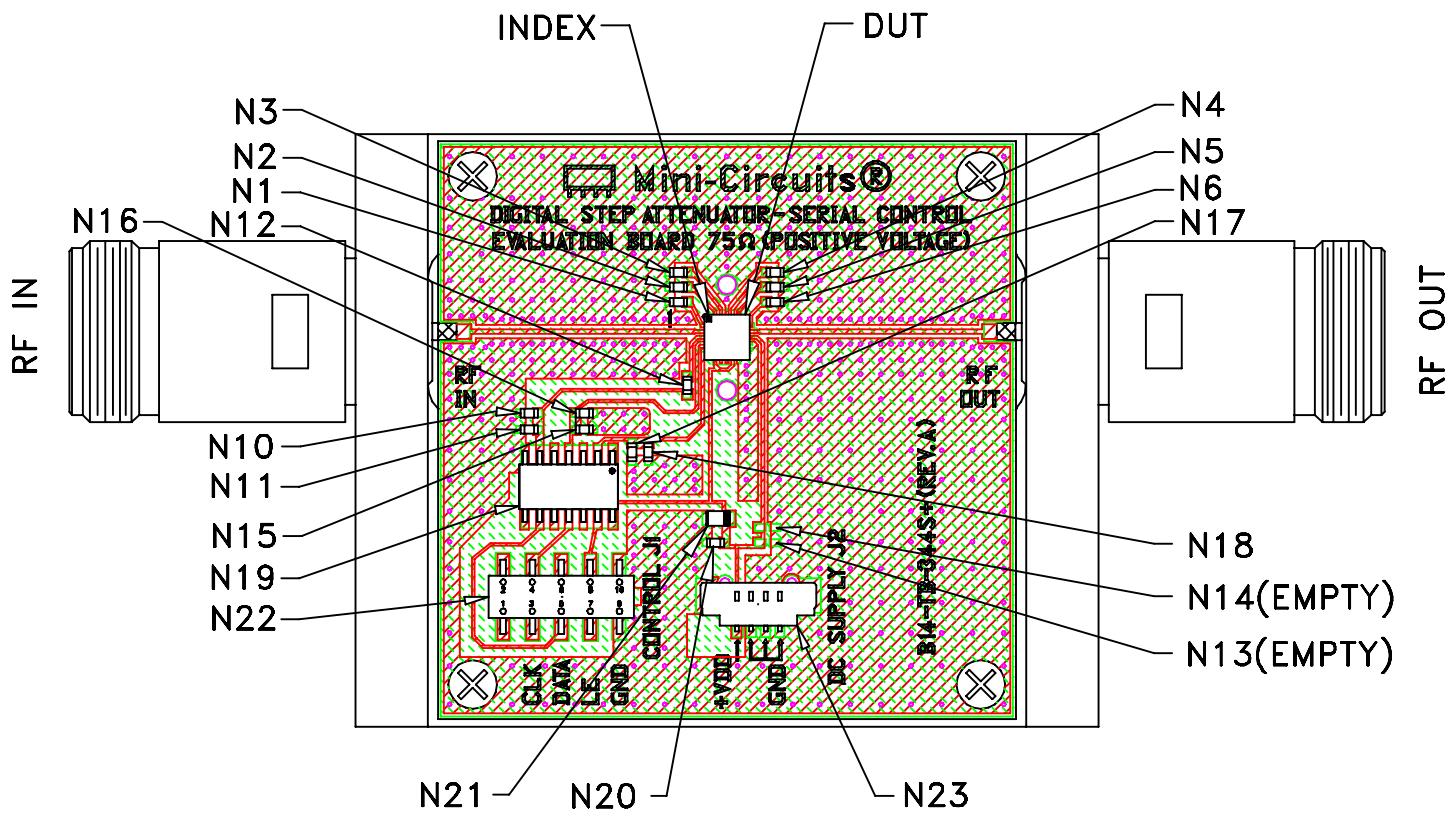


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13 Neptune Avenue
Brooklyn NY 11235PL, qm, DG983-1
TB-344 (75 Ω)

SIZE	CODE IDENT	DRAWING NO:	REV:
A	15542	98-PL-203	B
FILE: 98PL203	SCALE: 7:1	SHEET: 1	OF 1

Evaluation Board and Circuit



TB-344

Notes:

1. N-Type Female connectors.
2. PCB Material: FR4 Grade IT 180TC (ITEQ Corporation) or equivalent, Dielectric Constant=4.7, Thickness=.025 inch.

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Environmental Specifications

ENV33T1

All Mini-Circuits products are manufactured under exacting quality assurance and control standards, and are capable of meeting published specifications after being subjected to any or all of the following physical and environmental test.

Specification	Test/Inspection Condition	Reference/Spec
Operating Temperature	-40° to 85° C or -40° to 105° C Ambient Environment	Refer to Individual Model Data Sheet
Storage Temperature	-55° to 100° C or -65° to 150° C Ambient Environment	Refer to Individual Model Data Sheet
Temperature Humidity Bias	85°C, 85% RH, 96 hours	JESD22-A101B
Thermal Shock	-55° to 100°C, 100 cycles	MIL-STD-202, Method 107, Condition A-3, except +100°C
Solder Reflow Heat	Pb-Free Process: 260°C peak	J-STD-020, Table 4-1, 4-2 and 5-2; Figure 5-1
Solderability	10X magnification, 95% coverage	JESD22-B102, Method 1: Dip and Look Test
Marking Resistance to Solvents	Laser marked, visual observation	Mini-Circuits D4-Q4T0-04